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PAPERS

A triple path noise cancellation LNA with transformer output using 45 nm CMOS technology

Dheeraj Kalra[1,2], Vishal Goyal[2], Mayank Srivastava[1]

A triple path dual resistive feedback noise cancellation (TP-DRNC) low noise amplifier (LNA) with transformer output presented which provides high gain, low noise figure (NF), and high figure of merit (F_{M}). The analysis of triple path, dual resistive, gain, and NF have been discussed. The effect of various components used in the circuit have been analyzed and their optimized values are obtained which resulted in the high (F_{M}). The combination of dual resistive feedback with triple path NC transformer output allowed for low NF and high gain. The proposed GPDK 45 nm complementary metal oxide semiconductor (CMOS) technology-based LNA offers a flat gain curve of 10.81 dB over the range of 1.6 GHz to 4.3 GHz, or 2.7 GHz bandwidth, and S_{11} less than -9 dB. The input third order intercept point (IIP3) for the given bandwidth has value of 5.7 dBm, while the minimal NF achieved is 2.7 dB; (F_{M1}) is 14.026 and (F_{M2}) is 12.48. The proposed LNA's layout with an off-chip transformer has an area of 0.01985 mm^2

K e y w o r d s: LNA, noise cancellation, common gate-common source, resistive feedback, IIP3, noise factor (NF)

1 Introduction

A receiving circuit that can function at low voltage for energy harvesting and has a compact area is required for receiver systems [1]. In many different applications, including environment monitoring, farm settings, health monitoring, and wireless networks are highly demanded [2]. The supply voltage need is falling as technology results in small feature size. Decreasing the feature size of CMOS technologies can affect their performance in terms of velocity saturation, output impedance reduction, and mobility deterioration. Wideband LNA for various frequency ranges should use little power and have a small size needed for Internet of Things (IoT) applications. The receiver circuits subsequent blocks performances determined by the frontend wideband LNA [3]. After the band pass filter or immediately after the antenna, the LNA is attached. Low NF to lessen the impact of noise and strengthen the signal, a low reflection coefficient is required to reduce return losses, low power consumption to prolong battery life, and a small footprint to allow for the integration of more components on a single chip are all characteristics that an LNA should have. Since the LNA characteristics have tradeoffs, the total F_{M} should be high. One method to increase the LNA parameters is the distributed amplifier [4], which consists of MOS linked in a cascade arrangement with a gain of $A_{\mathrm{V}} = (g_{\mathrm{m}} R_{\mathrm{L}} N/2)^2$, where g_{m} is the MOS transconductance, R_L is the load, and N is the total number of MOS stages. Although it benefits from high gains, it also suffers from greater losses, high NF, and a wide area. Common gate (CG) [5] is another approach that aids in lowering input return loss. However, this topology has the draw-

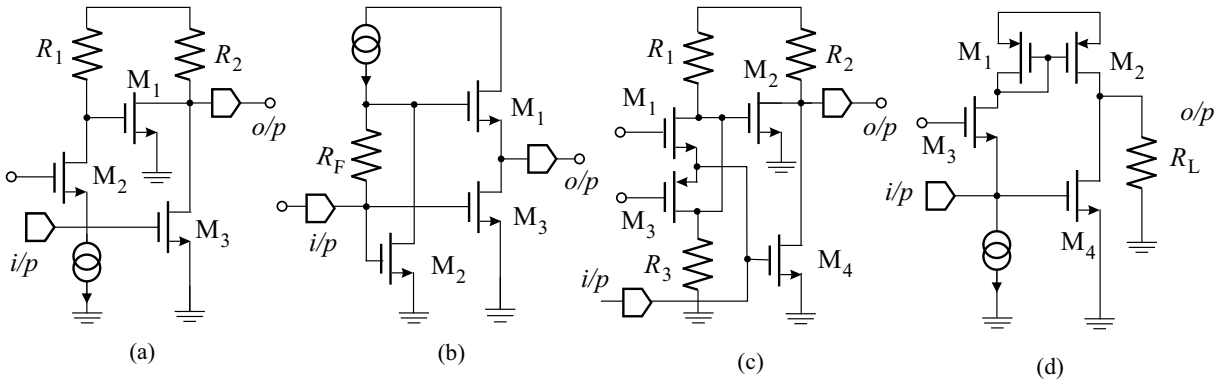

Fig. 1. (a) – CG NC LNA, (b) – resistive feedback NC, (c) – CG with stacked PMOS-NMOS, (d) – CG current mirror

[1] Department of ECE, National Institute of Technology, Jamshedpur, Jharkhand 831014, India dheeraj.kalra@gla.ac.in, mayank.ece@nitjsr.ac.in, [2] Department of ECE, GLA University, Mathura, Uttar Pradesh 281406, India, vishal.goyal@gla.ac.in

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back of a low g_{m} value and a high NF, which is calculated as $1+(\gamma g_{\mathrm{d0}})/(g_{\mathrm{m}}^2 R_{\mathrm{s}})$, where R_{s} is source resistance, γ is thermal noise coefficient, and g_{d0} is the output conductance ratio of i_{d} and v_{ds}. As NF is constrained by g_{m}, it is unable to rise further owing to a restriction on power consumption and cannot drop due to restriction on gain. Another method to reduce the NF is noise cancellation, in which the common source (CS) stage and CG stage at the output generate a 180° phase difference signals. To eliminate noise and increase gain, combine the two at the output.

Dual path [6] and triple path [7] techniques for NC are currently available. In two-path NC, resistive feedback NC [8]; shown in Fig. 1(b) gives low NF and high gain but has the drawback of having a low IIP3 of −4 dBm. In contrast, CG NC [6] gives a low gain of 9.7 dB, low IIP3 −6.2 dB, and 4.5 dB high NF. Leakage and intermodulation typically suppressed due to the enhanced presence of neighboring blocks on the transmitter chip.

Third-order harmonics produced within the range of interest because of the intermodulation of several high-order harmonics. Figure 1(c) depicts the CG stacked PMOS, NMOS topology [9], which uses NMOS-PMOS to match input impedance with NC to achieve high IIP3 but with constrained bandwidth. Nonlinear distortion components produced by PMOS-NMOS cancel out at the output, increasing IIP3. The MOS-generated channel noise travels through different paths at the output and cancels out its effects. Figure 1(d) depicts CG with a current mirror [10], which has good IIP3 but less voltage headroom and a supply voltage of 2.2 V, which results in high power consumption. Less voltage headroom in [10] is caused by transistors connected in the current mirror cascade, which forces the use of a high 2.2 V supply voltage; the reported bandwidth is 1.9 GHz.

In this paper, TP-DRNC LNA with transformer output network is proposed to minimize noise figure and increase gain for wideband. The concept of TP-DRNC LNA is given along with the mathematics for input matching, gain calculation, and NF calculation showing the effect of various component values. The proposed TP-DRNC LNA simulation is presented, and performance parameters are also investigated. The layout of the proposed LNA is presented along with a comparison table with the state of art given.

2 Proposed LNA circuit

Figure 2 shows the schematic of the proposed TP-DRNC LNA. Here, $M_{1\mathrm{P}}$ and $M_{2\mathrm{N}}$ are PMOS and NMOS connected in the complementary stages [11] in current reuse with PMOS $M_{5\mathrm{P}}$ and NMOS $M_{6\mathrm{N}}$, R_{F1} a feedback resistor helps break the dependency on the ratio of device dimension for $M_{1\mathrm{P}}$ and $M_{2\mathrm{N}}$. The power efficiency also gets improved by keeping the dimension (W/L) ratio of $M_{1\mathrm{P}}$ and $M_{2\mathrm{N}}$ as 1:1 and it provides enough value of g_m to get the input matching at 50 Ω. Another feedback resistor R_{F2} is also helpful in maintaining the linearity as well as sustaining the output matching at 50 Ω. The effect of R_{F1} and R_{F2} on the input matching, output matching, gain, and NF is presented in the further sections, and based on that the optimized values is obtained. Inductor L_1 used to cancel out the effect of MOS parasitic capacitances and therefore wide bandwidth is obtained. C_1 and C_2 capacitors used to block the DC components for further stages. M3P and M4N use the current reuse technique [12, 13] and provide a third path for noise cancellation. The dimensions of components used in the proposed LNA, given in Tab. 1.

2.1 Noise analysis

Figure 2 demonstrates the concept of the triple path noise cancellation technique applied in the proposed LNA. Two opposite phase noises generated at the source and drain of M1P. Noise part of I_{pM1} passed through Path A produces opposite phase noise at the drain of $M_{5\mathrm{P}}$ to noise at node X. In the same manner, Path C provides 180° phase difference noise at the drain of $M_{6\mathrm{N}}$. The noise through Path B gives an opposite phase as it get passed through the common source configuration. The noise I_{pM1} through paths A and C canceled by noise through path B. Noise from all sources of proposed LNA analyzed to get the exact calculation of NF. The noise factor of LNA is given as

$$N_{\mathrm{F}} = 1 + \sum_{i=1}^{6} F_{\mathrm{M}i} + F_{\mathrm{R_{F1}}} + F_{\mathrm{R_{F2}}}\,, \tag{1}$$

where $F_{\mathrm{M}i}$ is the noise contribution of all the six MOS, $F_{\mathrm{R_{F1}}}$, $F_{\mathrm{R_{F2}}}$ are the noise contribution by R_{F1} and R_{F2} respectively. MOS M_1 channel thermal noise at drain and source is

$$I_{n\mathrm{M_1}}^2 = 4K_{\mathrm{B}}T\frac{\gamma}{\alpha}g_{\mathrm{m1}}\,, \tag{2}$$

where T is absolute temperature, K_B is Boltzmann's constant, γ is thermal noise parameter whose value is 2/3 for long channel devices and greater than 1 for short channel devices, and α is the ratio of MOS transconductance and drain conductance at zero bias $g_{\mathrm{m1}}/g_{\mathrm{d0}}$, $g_{\mathrm{m}i}$ is the transconductance of i-th MOS.

Further

$$F_{\mathrm{M_1}} = \frac{I_{n\mathrm{outM_1}}^2}{4K_{\mathrm{B}}TR_{\mathrm{S}}G_{\mathrm{m}}^2}\,, \tag{3}$$

where R_S is source resistance and G_m is the equivalent transconductance.

Using abbreviations $g_{ij} = g_{mi} + g_{mj}$ and $g_{\mathrm{S}} = 1/R_{\mathrm{S}}$ and $g_{\mathrm{F1}} = 1/R_{\mathrm{F1}}$, $g_{\mathrm{F2}} = 1/R_{\mathrm{F2}}$

$$F_{M_1} = F_{M_2} = \frac{\gamma}{\alpha}\Big[\frac{g_{12}}{R_{\mathrm{S}}G_m^2}\Big]\times \times\left[\frac{g_{\mathrm{F2}}g_{56} + g_{34}\Big(\frac{g_{\mathrm{S}}}{g_{\mathrm{F2}}} + \frac{g_{\mathrm{F2}}}{g_{\mathrm{F1}}} + 1\Big)}{g_{12} + g_{\mathrm{S}} + g_{\mathrm{F2}}}\right], \tag{4}$$

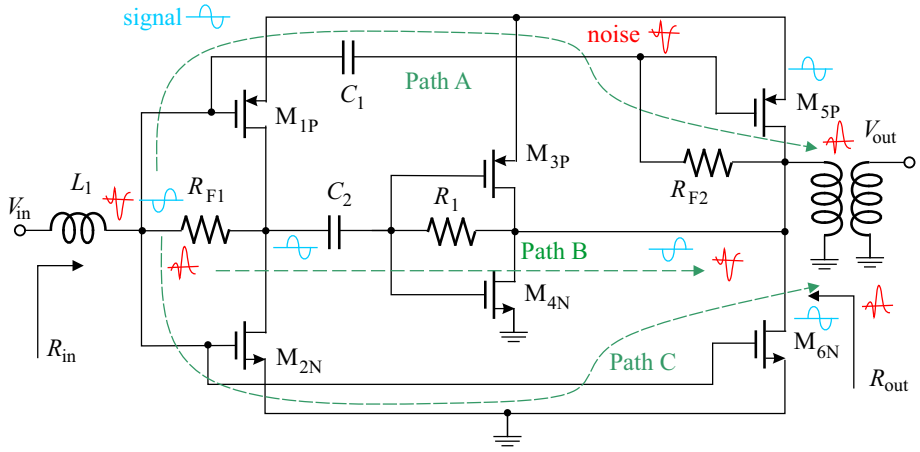

Fig. 2. Proposed TP-DRNC LNA with transformer output network

Table 1. Component dimensions used in Proposed LNA

Components	M_{1P} μm/nm	M_{2P} μm/nm	M_{3P} μm/nm	M_{4P} μm/nm	M_{5P} μm/nm	M_{6P} μm/nm	L_1 (nH)	R_{F1} (kΩ)	R_{F2} (Ω)	C_1 (pF)	C_2 (pF)	R_1 (kΩ)
Dimension	90/180	90/180	30/180	30/180	240/60	70/60	1.8	1.3	825	15	20	15

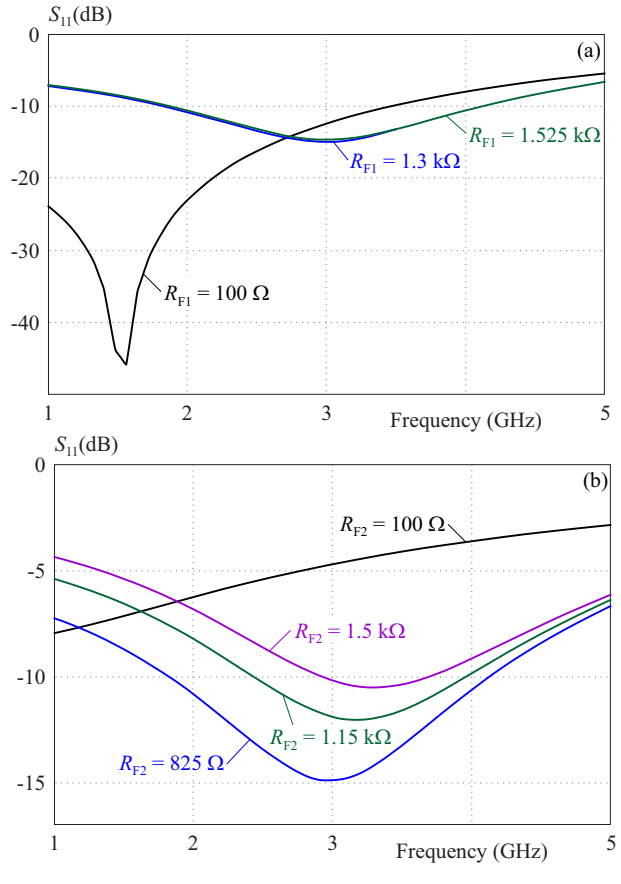

Fig. 3. Effect on S_{11} : (a) – of R_{F1}, and (b) – of R_{F2}

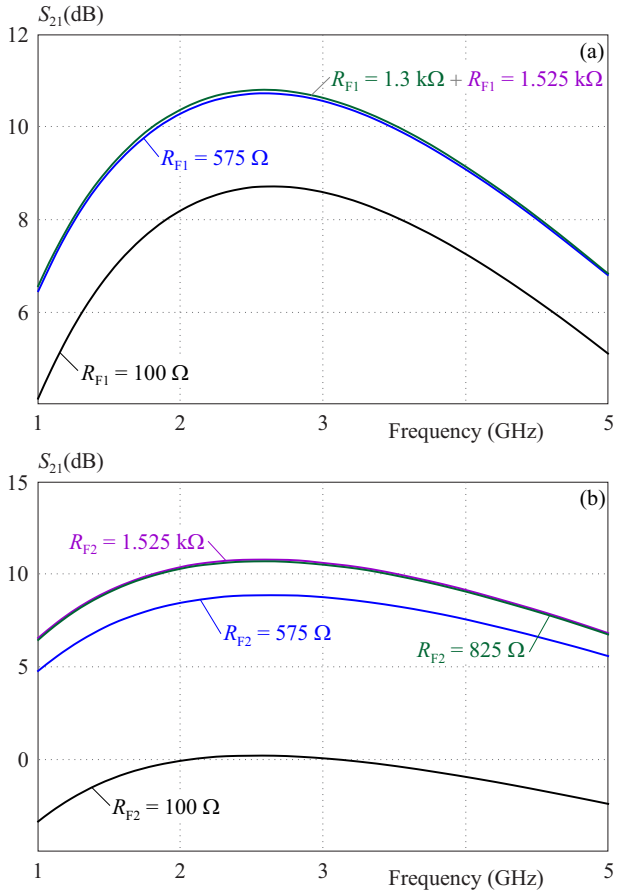

Fig. 4. Effect on S_{21} of: (a) – R_{F1}, (b) – of R_{F2}

$$F_{M_3} = F_{M_4} = \frac{\frac{\gamma}{\alpha} g_{34}}{R_S G_m^2}, \tag{5}$$

$$F_{M_5} = F_{M_6} = \frac{\frac{\gamma}{\alpha} g_{56}}{R_S G_m^2}, \tag{6}$$

Table 2. Comparison of the proposed work with other papers

Parameters	Proposed work	[14] MWCL (2009)	[15] TCASI (2012)	[16] TMTT (2012)	[17] MWCL (2015)	[18] TMTT (2019)	[19] JSSC (2021)
3dB BW (GHz)	$\boxed{1.6-4.3}$	0.1-20	DC-10	0.3-0.92	0.1-2.5	0.3-4.4	0.02-4.5
N_{F} (dB)	$\boxed{2.7}$	3.3-5.5	2.7-3.3	2-3.7	1.7-2.7	3-4.4	2.09-3.2
Peak Gain (dB)	$\boxed{10.8}$	12.7	10.5	21	18	26.7	15.2
P_{d} (mW)	$\boxed{8}$	12.6	13.7	3.6	13	13.9	4.5
Technology (nm)	$\boxed{45}$	90	65	180	65	65	28
Supply (V)	$\boxed{1.2}$	1.2	1	1.8	1.2	1	1
IIP3 (dBm)	$\boxed{5.7}$	-1	-3.5	-3.2	0	-14.2	-3.53
Area (mm^2)	$\approx\boxed{0.02}$	0.12	0.02	0.33	0.008	0.009	0.03
F_{M1}	$\boxed{14.1}$	13.5	1.9	-2	9.7	-12.3	12.3
F_{M2}	$\boxed{12.5}$	12	2	-7.1	8.1	-12.3	12.3

$$F_{R_{\mathrm{F1}}} = \frac{1}{R_{\mathrm{F1}} R_{\mathrm{S}} G_{\mathrm{m}}^2} \times$$
$$\times \left[1 + \frac{g_{34}\big(R_{\mathrm{F1}} || r_{01}\big)\big(g_{\mathrm{F1}} - g_{12}\big) - g_{56} - g_{\mathrm{F2}}}{g_{\mathrm{F1}}\Big[\big(R_{\mathrm{F1}} || r_{01}\big)\big(g_{\mathrm{F1}} - g_{12}\big) - 1\Big] - g_{\mathrm{F2}} - g_{\mathrm{S}}}\right], \quad (7)$$

2.2 Input matching

Proposed TP-DRNC LNA has input resistance as given in equation (8). The inductor L_1 connected at the input helps in improving the input matching. For low value of L_1, the matching is poor. The bandwidth increases with an increase in the value of L_1 but get shifted toward the lower frequency after certain values.

The optimum value of L_1 obtained is 1.8 nH for bandwidth is $4.31.6 = 2.7\,\mathrm{GHz}$ having S_{11} value lesser than 9 dB. The input port is matched at $50\,\Omega$ resistance.

$$R_{\mathrm{in}} = \frac{g_{34}}{g_{12} g_{34}\left[1 + g_{\mathrm{F2}}/g_{\mathrm{F1}}\right] + g_{56} g_{\mathrm{F2}}}. \quad (8)$$

Proposed TP-DRNC LNA has voltage gain given by

$$G = G_m R_{\mathrm{o}}\,, \quad (9)$$

where G_{m} is the overall transconductance of LNA and R_{o} is the output resistance

$$G_m = g_{34}\Big(1 - \frac{g_{\mathrm{m1}} + g_{\mathrm{m2}}}{g_{\mathrm{F1}}}\Big) - \Big(g_{56} - g_{\mathrm{F2}}\Big), \quad (10)$$

$$R_{\mathrm{o}} = \frac{1}{g_{34} + g_{\mathrm{F2}}} \simeq \frac{1}{g_{34}}\,. \quad (11)$$

The output port matched for the $50\,\Omega$ resistance. Henceforth gain is given by

$$G = 1 - \frac{g_{\mathrm{m1}} + g_{\mathrm{m2}}}{g_{\mathrm{F1}}} - \frac{g_{56} - g_{\mathrm{F2}}}{g_{34}}. \quad (12)$$

Figure 3(a) reviels the effect of R_{F1} on the input matching. As predicted by (8), the higher value of R_{F1} leads to the lower S_{11}, see Fig. 3(a). The optimum value of R_{F1} is $1.3\,\mathrm{k}\Omega$ while a higher value of R_{F1} leads to lowering the gain, Fig. 3(a). As R_{F1} increases towards a certain value, matching gets poor. The effect of R_{F1} on S_{11} is shown in Fig. 3(b), the high value leads to poor reflections henceforth optimal value for R_{F1} is $825\,\Omega$.

2.3 Gain

Figure 4 shows the effect of variation of R_{F1} and R_{F2}, on parameter S_{21}. The optimum value obtained for R_{F1} and R_{F2} are $1.3\,\mathrm{k}\Omega$ and $825\,\Omega$, respectively. Higher value of R_{F1} helps in achieving the high gain under the proper input matched conditions. As dictated from equation (12), small value of R_{F1} will be giving less gain which as indicated in Fig. 4(a). Smaller value of R_{F2} will provide less gain as depicted in Fig. 4(b). For $R_{\mathrm{F2}} = 100\,\Omega$, the gain is less while proposed LNA gives a high gain for $R_{\mathrm{F2}} = 825\,\Omega$ at relatively flat curve in entire bandwidth.

3 Simulation results

Simulation results for N_{F}, S_{11}, S_{21} and S_{22} are in Fig. 5. As demonstrated, the minimum value of N_{F} is 2.7 dB at 1.6 GHz, while the curve around value of 3.6 dB at 4.3 GHz – is relatively flat in the 2.7 GHz band. Input reflection coefficient S_{11} was simulated for the frequency range of 1 GHz to 5 GHz and we obtained the bandwidth values of 2.7 GHz at a lower 3 dB frequency of 1.6 GHz and upper 3 dB frequency of 4.3 GHz, with a minimum value of S_{11} 14.89 dB for 3.1GHz. The flat gain curve achieved for the given LNA architecture; attained the maximum value of 10.81 dB at 2.5 GHz and flat for the entire bandwidth of 2.7 GHz. It is important to reduce the reflection at the output terminal, and its value is 17.36 dB at 3.5 GHz for $50\,\Omega$ matching.

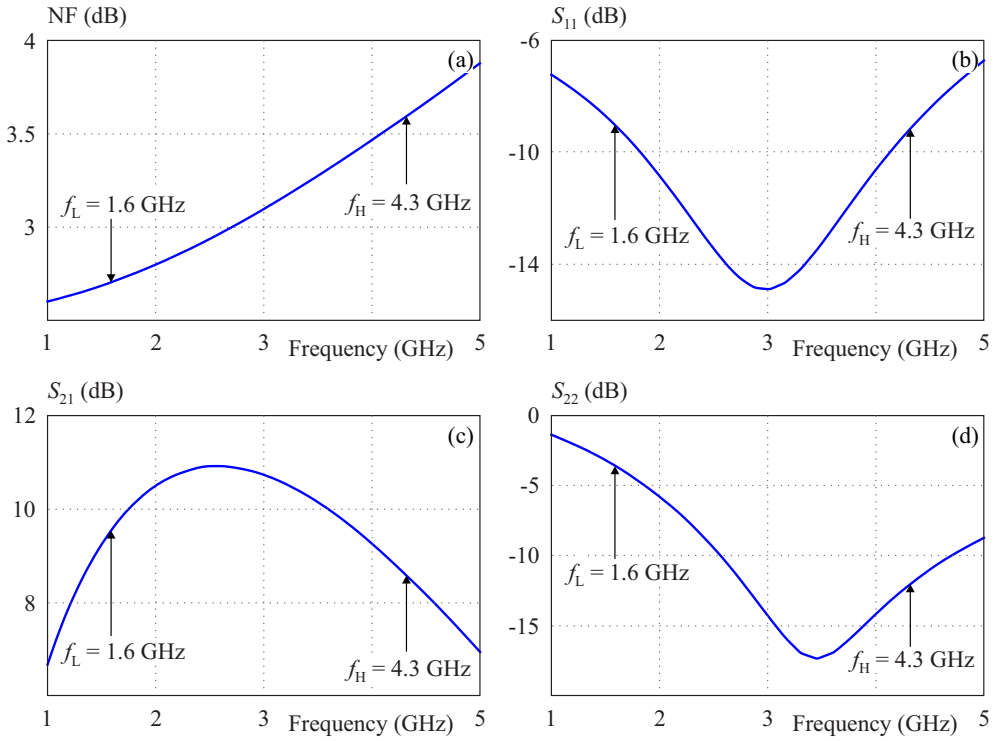

Fig. 5. Simulation results for: (a) – N_F, (b) – S_{11}, (c) – gain-S_{21}, (d) – S_{22} for the RF

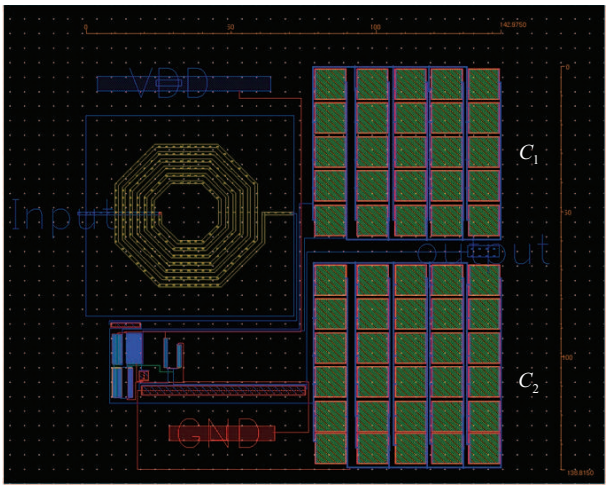

Fig. 6. Proposed TP-DRNC LNA layout with off-chip transformer

The overall evaluation of LNA using

$$F_{M1} = 20\log_{10}\left(\frac{P_3 S_{21} B_W}{P_d(N_F - 1)}\right), \tag{13}$$

comprises (P_3) - IIP3 value, maximal gain S_{21}, minimal N_F all in dB, maximal bandwidth B_W/GHz, and dissipation P_d/mW.

On the other hand another formula (including supply voltage parameter $v = V_{DD}/V$, [20] is also used to compare LNA's overall performance

$$F_{M2} = 20\log_{10}\left(\frac{P_3 S_{21} B_W}{vP_d(N_F - 1)}\right). \tag{14}$$

Table 2 compares the proposed LNA's success to those of other papers. The layout of proposed LNA with off chip transformer, depicted in Fig. 6 and clearly shows the area of $\approx 142\ \mu m \times 139\ \mu m$ *ie* 0.0197 mm^2. Here C_1 and C_2 are the blocking capacitors.

4 Conclusion

This paper presents a TP-DRNC LNA with a transformer matching at the output to increase the bandwidth. The triple path NC helped in achieving the low NF for the 2.7 GHz bandwidth. Mathematical analysis for NF, gain, and input resistance done and verified through the results. The gpdk 45 nm CMOS-based proposed LNA has the bandwidth of 2.7 GHz for S_{11} lesser than -9 dB and a flat gain of 10.81 dB for the band of 1.6 GHz to 4.3 GHz *ie* 2.7 GHz bandwidth. Proposed LNA has input matching of 50 Ω and transformer secondary winding terminated at 50 Ω also. The minimum NF obtained for the 2.7 GHz band is 2.7 dB; the resulting F_{OM1} is 14.064 and F_{OM2} is 12.48. The proposed LNA is having an area appriximately of 0.0197 mm^2 with an off-chip transformer. The comparison has been done with the latest references and proved the overall good performance of proposed LNA.

References

[1] B, Razavi, *Design of Analog CMOS Integrated Circuits*, New York: Tata McGraw Hill, 2016.

[2] A. Chaturvedi, M. Kumar, R. S. Meena, and G. K. Sharma, "Wideband ring mixer for band #1 of MB-OFDM systems in 180 nm CMOS technology", *Journal of Electrical Engineering*, no. 5, pp. 323–329, 2021.

[3] A. Shukla, "Intelligent reflected surfaces assisted code domain non-orthogonal multiple access scheme", *Journal of Electrical Engineering*, no. 5, pp. 343–347, 2021.

[4] F. Zhang and P. R. Kinget, "Low-power programmable gain CMOS distributed LNA", *IEEE Journal of Solid-State Circuits*, no. 6, pp. 1333–1343, 2006.

[5] M. Kumar and V. K. Deolia, "A wideband design analysis of LNA utilizing complimentary common gate stage with mutually coupled common source stage", *Analog Integrated Circuits and Signal Processing*, no. 3, pp. 575–585, 2019.

[6] C.-F. Liao and S.-I. Liu, "A Broadband Noise-Canceling CMOS LNA for 3.1–10.6-GHz UWB Receivers", *IEEE Journal of Solid-State Circuits*, no. 2, pp. 329–339, 2007.

[7] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A 0.096 mm2 1–20-GHz Triple-Path Noise-Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration", *IEEE Transactions on Microwave Theory and Techniques*, no. 1, pp. 144–159, 2020.

[8] H. Yu, Y. Chen, C. C. Boon, C. Li, P.-I. Mak, and R. P. Martins, "A 0.044-mm^2 0.5-to-7-GHz Resistor-Plus-Source-Follower -Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3± 0.45 dB", *IEEE Transactions on Circuits and Systems II: Express Briefs*, no. 1, pp. 71–75, Jan 2019.

[9] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation", *IEEE Journal of Solid-State Circuits*, no. 5, pp. 1164–1176, 2008.

[10] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A Wideband Noise-Canceling CMOS LNA With Enhanced Linearity by Using Complementary nMOS and pMOS Configurations", *IEEE Journal of Solid-State Circuits*, no. 5, pp. 1331–1344, 2017.

[11] J. Chang and Y. Lin, "0.99 mW 3-10 GHz common-gate CMOS UWB LNA using T-match input network and self-body-bias technique", *Electronics Letters*, no. 11, pp. 658–659, 2011.

[12] S. V. Ankathi, S. Athukuri, S. Mohan, K. Balamurugan, and M. N. Devi, "A 5–7 GHz current reuse and gm-boosted common gate low noise amplifier with LC based ESD protection in 32 nm CMOS", *Analog Integrated Circuits and Signal Processing*, pp. 573–589, 2017.

[13] Y.-T. Chang and H.-C. Lu, "A V-Band Low-Power Digital Variable-Gain Low-Noise Amplifier Using Current-Reused Technique With Stable Matching and Maintained OP1dB", *IEEE Transactions on Microwave Theory and Techniques*, no. 11, pp. 4404–4417, 2019.

[14] M. Chen and J. Lin, "A 0.1–20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS", *IEEE Microwave and Wireless Components Letters*, no. 5, pp. 323–325, 2009.

[15] K.-H. Chen and S.-I. Liu, "Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique", *IEEE Transactions on Circuits and Systems I: Regular Papers*, no. 2, pp. 305–314, Feb 2012.

[16] S. Woo, W. Kim, C.-H. Lee, H. Kim, and J. Laskar, "A Wideband Low-Power CMOS LNA With Positive–Negative Feedback for Noise, Gain, and Linearity Optimization", *IEEE Transactions on Microwave Theory and Techniques*, no. 10, pp. 3169–3178, 2012.

[17] H. Lee, T. Chung, H. Seo, I. Choi, and B. Kim, "A Wideband Differential Low-Noise-Amplifier With IM3 Harmonics and Noise Canceling", *IEEE Microwave and Wireless Components Letters*, no. 1, pp. 46–48, 2015.

[18] J. Jang, H. Kim, G. Lee, and T. W. Kim, "Two-Stage Compact Wideband Flat Gain Low-Noise Amplifier Using High-Frequency Feedforward Active Inductor", *IEEE Transactions on Microwave Theory and Techniques*, no. 12, pp. 4803–4811, 2019.

[19] A. Bozorg and R. B. Staszewski, "A 0.02–4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse", *IEEE Journal of Solid-State Circuits*, no. 2, pp. 404–415, 2021.

[20] P. B. T. Huynh, J.-H. Kim, and T.-Y. Yun, "Dual-Resistive Feedback Wideband LNA for Noise Cancellation and Robust Linearization", *IEEE Transactions on Microwave Theory and Techniques*, no. 4, pp. 2224–2235, 2022.

Dheeraj Kalra obtained his master degree in information and communication technology from GLA University, Mathura, India. He is currently pursuing PhD from NIT Jamshedpur, India. His areas of interest include Radio Frequency Integrated Circuit Design and other latest trends in technology. He has more than 11 years of experience in teaching and research in integrated circuits.

Vishal Goyal is a senior member IEEE, received his BE degree in Electronics engineering from Nagpur University, India in year 2001 and MTech degree in Digital Communication from Uttar Pradesh Technical University, Lucknow in year 2006. He received his PhD degree from GLA University, Mathura in year 2016. His research interests include nonlinear control, adaptive control and sliding mode control, process control, evolutionary algorithms, RF Integrated Circuits and intelligent systems.

Mayank Srivastava obtained PhD in analog integrated circuits and signal processing from Jamia Millia Islamia, New Delhi, India, in 2015. Presently he is working as an Assistant Professor with Department of Electronics and Communication Engineering, National Institute of Technology, Jamshedpuer, India. His research interest is in the areas of analog circuits. Dr. Srivastava has authored or co-authored 50 research papers in SCI/Scopus indexed International Journals and Conferences. He acted as reviewer of various SCI Indexed international journals and worked as a member of Technical Program Committee/ Reviewer/ Session Chair in several international conferences in India and abroad.

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