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Elementary design and analysis of QCA-based T-flipflop for nanocomputing

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This work presents a new T-flipflop design based on quantum-dot cellular automata technology, with the standard two inputs (T and clock) and two outputs (Q and $\bar{Q}$). It adheres to the typical QCA layout design approach, which consists of two majority voters and one inverter (to produce the complementary output, $\bar{Q}$). It is a single-layered design with no crossover. A memory loop is used to retain previous values and aid the toggling operation of the T-flipflop. This design achieves improved functionality and reduced area requirement compared to existing designs. In addition, the study investigated energy loss and cost functions. In particular, the total energy loss is reduced by 10% and 22% compared to the best design when analyzed with the QCAPro and QCADesigner-E (QDE) tools, respectively. The area-delay and energy-delay cost functions outperform the best current design by 1.3 and 1.07 times, respectively. Overall, this work advances QCA-based flipflop (QTFF) designs and emphasizes the potential of QCA technology for creating effective QCA circuits.

Keywords: flipflop, T-flipflop, QCA, quantum dot cellular automata, QTFF

1 Introduction

Quantum dot cellular automata (QCA) is an emerging technology that holds great promise for revolutionizing the field of logic circuit design. With the relentless demand for smaller, faster, and more energy-efficient computing systems, researchers are constantly exploring alternative approaches to conventional technologies. QCA is one such alternative that leverages the principles of quantum mechanics to enable ultra-compact, high-performance logic circuits [1]. The heart of QCA is the quantum dot, a nanoscale structure capable of confining a small number of electrons [2]. When arranged in a regular array, these quantum dots can interact and exhibit unique quantum phenomena such as quantum tunneling and Coulomb blockade [3]. By harnessing these effects, QCA allows for manipulating and transmitting information through the collective behavior of quantum dots, paving the way for novel device architectures and logic gates [4]. A significant advantage of QCA is its inherent parallelism. In a QCA array, multiple bits of information can be processed simultaneously due to the collective interactions between quantum dots [5]. This parallelism enables the potential for highly efficient and parallel computing, which can lead to significant performance improvements in various applications. QCA also offers the promise of nonvolatility, meaning that QCA-based circuits retain their state even when power is turned off. This characteristic eliminates the need for power-consuming memory elements, such as flipflops, to store data. The nonvolatility of QCA can contribute to reduced power consumption and increased system reliability [2-3].

A cell, as depicted in Fig. 1(a), is the fundamental building block of QCA and is made up of four quantum dots and two extra free electrons that are able to pass across the dots. These two electrons keep a large distance apart because of the Coulomb repulsive force, resulting in two distinct configurations, as seen in Fig. 1(a). In the context of QCA, a wire is the grid of QCA cells used to route signals within a QCA circuit, as depicted in Fig. 1(b). QCA wires are essential components for interconnecting QCA cells and facilitating information transmission between different circuit nodes. A QCA inverter, also known as a QCA NOT gate, is a fundamental logic gate used to invert the logical state of a QCA cell. It takes an input signal and produces that input's logical complement (opposite), as shown in Figs. 1(c) and 1(d). A majority gate, also known as a majority voter (MV), is a logic gate that performs a majority function on multiple input signals. It takes multiple input signals (A, B, and C) and produces an output (F=AB+BC+CA) signal representing the majority logic state among the inputs, depicted in Fig. 1(e). The MV is a fundamental building block in QCA circuits and is used for various purposes. It can be used for logic operations like AND and OR and to create more complex circuits. QCA clocking refers to the process of generating and synchronizing clock signals in QCA circuits. Clock signals are used to regulate the timing of signal propagation, charge manipulation, and logic state transitions in the QCA circuit. Figure 1(f) shows a complete clock with four phases or zones.

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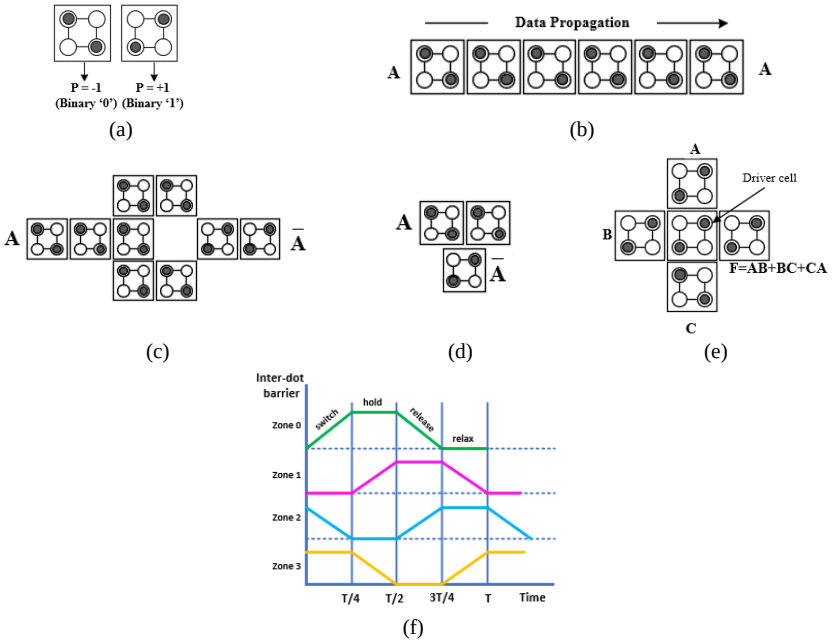


Fig. 1. QCA fundamentals: (a) cell structure, (b) wire, (c) basic inverter, (d) modern inverter, (e) MV, and (f) QCA clock zones

Table 1. Logic table of T-flipflop if memory $Q_n = 0$

Inputs		Outputs with $Q_n = 0$		Comments
Clock (*CK*)	*T*	Q_{n+1}	$\overline{Q_{n+1}}$	State
0	0	0 (as Q_n=0)	1	Hold
0	1	0	1	No change
1	0	0	1	Hold
1	1	1	0	Toggle

Following the introductory part in Section 1, the article continues with the following sections: A brief outline of the existing works on QTFF is discussed in Section 2. The proposed QCA design is discussed in Section 3. The simulation results are presented in Section 4. In section 5, the performance evaluations are included. Section 6 contains a comparison of this design to other existing designs. The conclusion of this work is presented in Section 7.

2 Existing works on QTFF

The design of QTFF is an active research area that offers promising opportunities for developing advanced nanoscale logic circuits. The literature on QTFF highlights various studies focusing on layout design, optimization, robustness analysis, etc. These research efforts contribute to the advancement of QCA technology and pave the way for future developments in QCA-based sequential logic elements. This section of this article explores the existing QTFFs, focusing on the key research efforts, challenges, and advancements in this area.

A QTFF of 55 cells is suggested and implemented in [9]. It has an area of 59004 nm^2. Two inverters and four MVs are used. The arrangement has a 6-clock zones (1.5-clock signals) delay. The article suggests a novel QTFF configuration and thoroughly examines its performance and usefulness, but the energy analysis part is absent. The work [10] focuses on improving the performance of QTFF by utilizing a memory loop for data storage. The layout has a total area of 56244 nm^2 and is created using 47 cells. Similar to the prior design [9], it makes use of four MVs, two inverters, and 6-clock zones (1.5-clock signals) for the circuit to function correctly. It includes energy estimation using the QCAPro tool, in contrast to earlier work [9]; however, QDE analysis is not included. This study investigates several design parameters and evaluates them against other designs to offer insightful information for future ideas. In [11], a QTFF that utilizes 43 cells and takes up 47124 nm^2 of area is proposed. It contains two inverters, four MVs, and a delay of 5-clock zones (1.25-clock cycles). This research investigates the utilization of MVs for implementing QTFF. The biggest drawback of this design is that it only has one input node, *T*, as a result of

the absence of the input node clock (*CK*). The work also excludes any consideration of energy estimation. However, another design with 28 cells is proposed at the same time, requiring a 56244 nm^2 area and having both the inputs *T* and clock (*CK*). Nevertheless, the gate count and delay remain the same; they include the use of two inverters, four MVs, and a delay of five clock zones (1.25-clock cycles). Energy analysis is missing for both designs in [11]. In [12], an unconventional QTFF with two inputs (in contrast to traditional) and a select line is described. The layout design makes use of 43 cells with an overall area of 47124 nm^2. Three MVs and one inverter make up the design, which has an input-output delay of five clock zones (1.15-clock cycles). It took into account the energy calculation made with QCAPro but not QDE. The design's biggest flaws are the multiple inputs and the absence of the T-input. A remarkable piece of work with a simple 21-cell QTFF structure has been presented in [13]. It requires 18644 nm^2 of space and has a delay of 6-clock zones (1.5 clock cycles). There are just two MVs and no inverter. It used QCAPro to analyze the energy dissipation. The fundamental drawback of the layout is the large input-to-output delay, which is very significant for a straightforward design. The work also ignored QDE-based analysis. In [14], a multiplexer-based T-flipflop without any MV is introduced. It takes up 13524 nm^2 and only needs 19 cells. It has a delay of 3-clock zones (0.75-clock cycle) and only utilizes one inverter. This structure's biggest flaw is that it lacks MV, making it challenging to compare to existing ones. Along with T-input, there is no clock signal, which is crucial for a QTFF. Additionally, no energy calculations are made for the suggested design. A QTFF is shown in [15] using 22 cells, two MVs, and no NOT gates. It takes up 17444 nm^2 and has a delay of 5-clock zones (1.25-clock cycles). A different QTFF architecture with 20 cells, two MVs, and one inverter is suggested here. The second design, which includes a delay of five clock zones (1.25-clock cycles), took up 18644 nm^2 of space. Both designs are outstanding examples of QTFF's work. It used QDE to calculate energy dissipation but disregarded QCAPro analysis. In 2023, a QTFF is proposed with 77 cells, 4 MVs, and 2 NOT gates [16]. It requires 105084 nm^2 of area and has a delay of 8-clock zones (2-clock cycles). This design has a number of drawbacks, including its large size, the existence of internal nodes, and the absence of an energy calculation.

There are benefits and drawbacks to each of the aforementioned designs. Therefore, this work aims to address major problems identified in the existing QTFFs. A straightforward loop-based QTFF without internal nodes is presented in this study. It has normal and complementary outputs, which none of the existing designs have considered. It investigated energy dissipation with QCAPro and QDE, which are missing in the literature on QTFF.

3 Proposed design

A standard QTFF has two inputs: *T* and clock (CK). The are two outputs: Q_{n+1} and $\overline{Q_{n+1}}$. Q_n is the memory value. Whatever the value of *T*, the output Q_{n+1} will be in the hold state Q_n, which is the memory value, while the clock (*CK*) is low (0). The output is once more in the hold state or memory Q_n when the clock is high (1) and *T* is low (0). The output Q_{n+1} will be in the toggle state $\overline{Q_n}$ when the clock *CK* and *T* are high, as shown in Table 1. In our work, the memory, or Q_n state, is zero.

Figures 2(a) and 2(b) depict the block diagram and layout of the proposed QTFF, respectively. The suggested QTFF has zero memory (Q_n=0). This architecture uses a loop to maintain memory and carry out the simultaneous "hold-no change-hold-toggle" operations to avoid the crossover requirement. It is a coplanar layout without any crossover. The suggested QTFF is far more efficient than the earlier designs, requiring just 19 QCA cells with a total area of 13524 nm^2 and a cell area of 5832 nm^2. Since a greater value of area utilization is advantageous, a 43% area utilization rate is fairly excellent. To produce complementary output, it makes use of a NOT gate. In addition, the main layout utilizes two MVs: One MV functions as an AND gate, while the other MV functions as an XOR gate. This work is driven by the layouts of [13] and [15]. The processing of input requires five clock zones (1.25-clock cycles). Hence the delay is 1.25-clock cycles. QCADesigner-2.0.3 is used to create the layout.

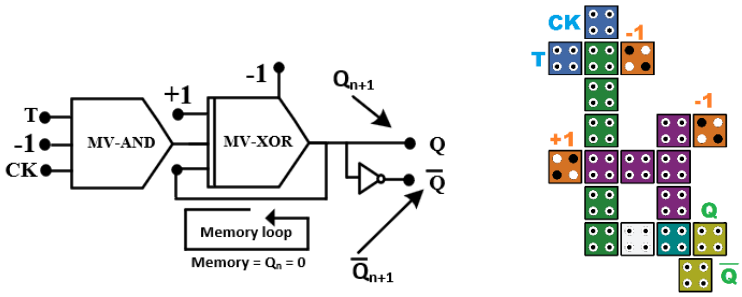


Fig. 2. Proposed QTFF: (a) block diagram, and (b) QCA layout

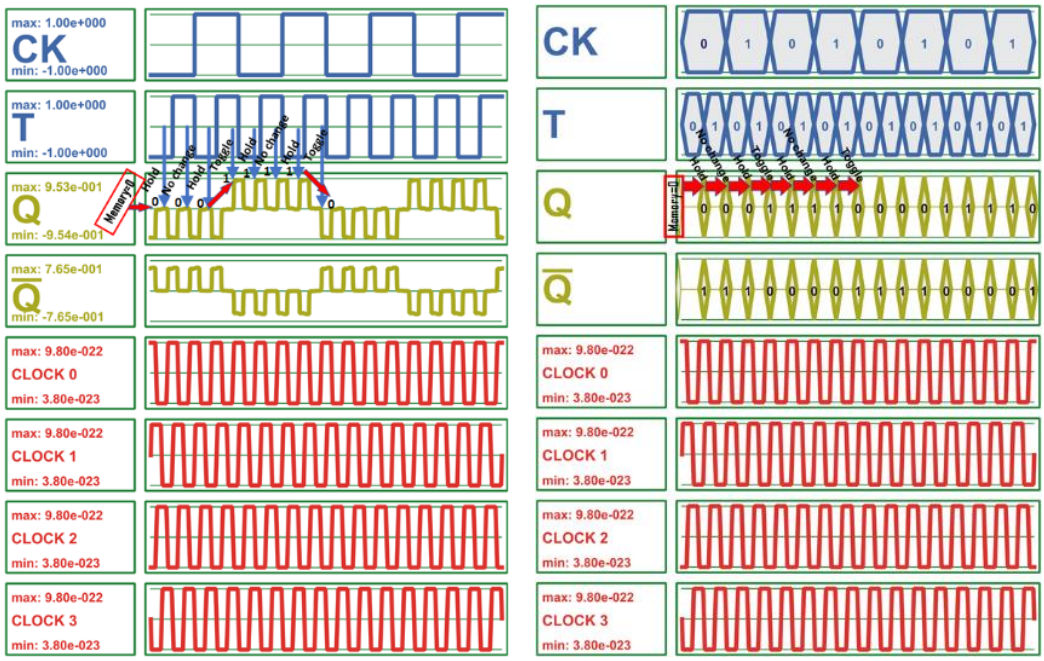


Fig. 3. Simulation results: (a) output in normal mode, and (b) output in bus mode

4 Simulation results

The simulation tool QCADesigner is used to design and test the suggested QTFF. As previously stated, it is assumed that the memory (Q_n) is 0. Similar to the digital T-flipflop, the QTFF is a form of flipflop that changes its output state dependent on the input signal when the clock signal changes from low to high. It is clearly visible in the output shown in Fig. 3(a) and Fig. 3(b).

When the clock input is low (0), the state of the QTFF remains unchanged, regardless of the T input value. So, if the T input is 0, the outputs Q and $\bar{Q}$ will stay at their previous state (as mentioned, the memory = 0); hence, Q = 0 and $\bar{Q}$ = 1. It is called the HOLD state. Similarly, if T = 1 with CK = 0, the outputs Q and $\bar{Q}$ will stay at their previous state; here the previous state is 0. Hence, Q = 0 and $\bar{Q}$ = 1. It is called the NO CHANGE state. When the clock input transitions from high, the QTFF evaluates the T input and toggles its output state accordingly. If the T input is 0 with CK = 1, the outputs remain the same as the previous state. So, Q and $\bar{Q}$ retain their previous values (Q = 0 and $\bar{Q}$ = 1). It is again a HOLD state. The outputs toggle their state if the T input is 1. As the previous state is 0 (Q = 0 and $\bar{Q}$ = 1), the QTFF changes its state to 1 (Q = 1 and $\bar{Q}$ = 0). It is the TOGGLE state. This cycle ends here with the value of T = 1.

In the next cycle, when the clock input is low (0) and the T input is 0, the outputs Q and $\bar{Q}$ will stay at their previous state (as mentioned, the previous stage value is 1); hence, Q = 1 and $\bar{Q}$ = 0. It is again HOLD state. Similarly, if T = 1 with CK = 0, the outputs Q and $\bar{Q}$ will stay at their previous states, here the previous state = 1. Hence, Q = 1 and $\bar{Q}$ = 0. It is a NO CHANGE state. If the T input is 0 with CK = 1, the outputs remain the same as the previous state. So, Q and $\bar{Q}$ retain their previous

values (Q = 1 and $\bar{Q}$ = 0). It is again a HOLD state. The outputs toggle their state if the T input is 1. As the previous state is 1 (Q = 1 and $\bar{Q}$ = 0), the QTFF changes its state to 0 (Q = 0 and $\bar{Q}$ = 1). It is again the TOGGLE state. The same procedure continues. As a result, the QTFF's operation is verified and identical to the truth table mentioned earlier.

5 Performance analysis of proposed QTFF

In the context of QCA circuits, performance analysis refers to the evaluation and assessment of various metrics and parameters that measure the efficiency and effectiveness of the circuit design. The performance analysis of the proposed design is mentioned below.

5.1 Design parameters analysis

In a QTFF, the design parameters play a crucial role in determining the performance and efficiency of the circuit. Let us analyze and evaluate some of the key design parameters for the suggested QTFF:

Cell complexity: Cell complexity refers to the total number of QCA cells required to construct the QTFF. A higher cell count may lead to increased area usage and potentially higher power consumption. The cell complexity of the proposed QTFF is 19.

Total area: The physical space that the entire circuit or device takes up is referred to as the total area. It includes the area taken up by layout, which is determined by the simulation tool QCADesigner. A lower overall area value is advantageous. The total area of the proposed QTFF is 13524 nm^2.

Cell area: The cell area is the area occupied by the QCA cells, excluding the layout's free spaces. It is better to have a smaller cell size. The cell area of the proposed QTFF is 5832 nm^2.

Area usage (%): Area usage refers to the measure of how efficiently the available layout area is utilized by QCA cells. It represents the ratio of the occupied cell area to the total layout area. A higher area usage indicates that the QCA layout is utilizing the total area more efficiently, leaving less space loss. On the other hand, a lower area usage suggests that a significant portion of the total area is blank, hence the loss of the signed area. A higher value of area usage is better for QCA technology but may require to increase in cell complexity. Hence, it is a challenge for a designer to optimize cell complexity and area usage. For QCA technology, a greater value of area utilization is beneficial, albeit it might necessitate a rise in cell complexity. As a result, making the cell complexity and area usage optimal is a challenge for the designer. The area usage of the proposed QTFF is 43%.

Delay: The number of clock zones applied from input to output in the worst root is referred to as the delay or latency of a QCA circuit. It is measured in clock cycles or clock zones. A full clock cycle is comprised of four clock zones. The delay of the proposed layout is 5-clock zones (1.25-clock cycles) since it employed five clock zones as "clock 0-clock 2-clock 0-clock 3-clock-2" in the worst root, starting from input T to output Q. A lower delay is desirable.

Number of gates: Two MVs have been employed in the proposed design. One MV functions as an AND gate, and the other MV functions as an XOR gate. There are no inverters used in the design. The use of MVs and inverters should be kept to a minimum.

5.2 Calculation of energy loss

One crucial aspect of QCA analysis is energy calculation, which helps evaluate the energy efficiency of QCA-based circuits. Energy loss in a QCA design can be estimated using two tools: QCAPro and QDE. QCAPro is a powerful simulation tool specifically designed for energy analysis of QCA designs. QCAPro provides several features and methodologies for accurately estimating energy consumption in QCA designs. Three different tunneling energy levels (0.5 E_K, 1.0 E_K, and 1.5 E_K) are used in the energy evaluation of QTFF, which is conducted at a temperature of 2.0 K. The suggested QTFF has an energy dissipation of 25.16 meV, 33.34 meV, and 43.51 meV over these three levels mentioned earlier. The simulation tool (QCAPro) creates an energy dissipation map and a polarization hotspot, as seen in Figs. 4(a) and 4(b), which provides an overall understanding of the energy dissipated by cells. More energy is lost when the cell color is darker. Similarly, a darker-colored polarization hotspot exhibits higher polarization values. QDE is a software tool specifically developed for modeling, simulating, and analyzing QCA designs. In addition to its comprehensive design capabilities, QDE provides features for calculating energy loss in QCA designs. The suggested QTFF has an average energy dissipation of 0.522 meV and a total energy dissipation of 5.74 meV, as measured by the QDE tool.

5.3 Calculation of cost functions

It is essential to compute the cost functions to make accurate performance assessments. The three most important cost functions – area delay cost (ADC), QCA-specific cost (QSC), and energy-delay cost (EDC) – can be calculated for the proposed QTFF.

The ADC (area $\times$ delay^2) is a metric representing the trade-off between the physical area occupied by a QCA circuit and its delay. In general, a smaller area and shorter delay are desirable, so a lower area-delay cost

indicates a more efficient circuit. The ADC for the proposed QTFF is 0.32.

The QSC ((MV^2 + NOT gate + wirecrossing^2) × delay^2) is a combination of multiple items that are considered to achieve a trade-off between different design factors. The cost function incorporates weighted terms for MVs, inverters, crossovers, and delay, allowing designers to optimize the circuit based on their priorities and design constraints. The calculated QSC for the proposed QTFF is 125.

The EDC (energy^2×delay^2) measures the energy consumption of a QCA circuit relative to its delay. A lower energy-delay cost indicates a more energy-efficient circuit. EDC for the proposed QTFF is 0.027 with QCAPro energy at γ=1.0 E_K and energy in eV.

6 Comparisons

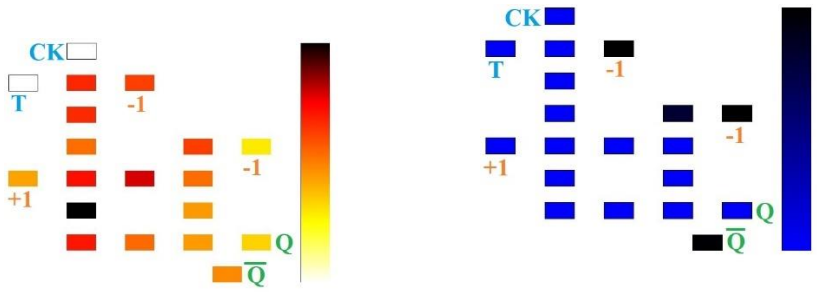
This section compares this work with existing works in the field. The aim is to demonstrate the unique contributions and advancements made by the proposed QTFF in comparison to previous works. The design of QTFF has been investigated in a number of pertinent studies [9–16], which have already been mentioned in the literature study. The work [14] cannot be compared to the proposed work because it employs a different layout design method and does not use an MV. There are various QTFFs that already exist that compete with the suggested design; nevertheless, while these earlier studies have contributed significantly, this work expands on their findings and presents several novel aspects. Firstly, the proposed layout of QTFF is similar to a digital T-flipflop in that it has two inputs (T and clock) and two outputs (Q and $\bar{Q}$). It is an MV-based layout with just one inverter used to invert the output Q and no internal inverters. It has a lower cell count than the best available design in [15] and better area usage, which suggests a less loss of overall area. According to Table 2, the overall area occupied is down 22.47% from the best design [15]. According to QCAPro and QDE analyses, the overall energy loss is reduced from the best design [13] by 10% and 22%, respectively, as shown in Tables 3 and 4. As indicated in Table 5, the cost function ADC is 1.3 times, and the cost function EDC is 1.07 times superior to the design [15]. Therefore, this paper compares the proposed T-flipflop design to other QCA based flipflop designs and assesses its performance using a range of benchmarks. The findings demonstrate that the proposed design out-performs the competition in terms of energy usage, cost, and space utilization. The introduction of a new layout, the focus on power loss, and the extensive performance evaluation all contribute to the novelty and relevance of this research. The findings pave the way for more efficient and high-performance QCA-based flipflops in future logic circuit designs.

Table 2. Comparison of design parameters

Work	Year	Cell count	Total area	Cell area	Area usage	Delay
[9]	2014	55	59004 nm^2	17820 nm^2	30%	6-clock zones
[10]	2015	47	56244 nm^2	15228 nm^2	27%	6-clock zones
[11]	2016	43	47124 nm^2	13932 nm^2	30%	5-clock zones
[11]	2016	28	32844 nm^2	9072 nm^2	28%	7-clock zones
[12]	2018	43	47124 nm^2	13932 nm^2	30%	5-clock zones
[13]	2019	21	18644 nm^2	6804 nm^2	37%	6-clock zones
[15]	2022	22	17444 nm^2	7128 nm^2	41%	5-clock zones
[15]	2022	20	18644 nm^2	6480 nm^2	35%	5-clock zones
[16]	2023	77	105084 nm^2	24948 nm^2	24%	8-clock zones
Proposed	2023	19	13524 nm^2	5832 nm^2	43%	5-clock zones

Table 3. Comparison of energy loss examined by QCAPro

Work	Leakage energy loss (meV)			Switching energy loss (meV)			Total energy loss (meV)		
	0.5 E_K	1.0 E_K	1.5 E_K	0.5 E_K	1.0 E_K	1.5 E_K	0.5 E_K	1.0 E_K	1.5 E_K
[9]	17.80	52.49	92.32	36.36	30.83	25.85	54.16	83.32	118.17
[10]	15.67	44.91	78.23	15.60	13.49	11.49	31.36	58.40	89.72
[11]	14.21	42.07	74.09	56.52	47.94	40.10	70.73	98.59	114.19
[11]	11.21	29.15	48.68	17.70	15.12	12.80	31.91	44.27	61.48
[12]	14.64	41.44	71.58	34.68	29.40	24.93	49.32	70.84	96.51
[13]	6.27	18.49	32.67	22.94	19.72	16.73	29.22	38.22	49.40
[15]	6.50	19.17	34.07	24.69	21.25	18.06	31.19	40.42	52.13
[15]	7.08	19.21	32.72	18.16	15.27	12.81	25.24	34.48	45.53
[16]	23.87	72.32	128.94	93.19	80.00	67.52	117.06	152.32	196.46
Proposed	5.67	16.97	29.83	19.49	16.37	13.68	25.16	33.34	43.51



(a) (b)

Fig. 4. QCAPro generated cell mapping of proposed QTFF at γ = 0.5 E_K, (a) energy hotspots, and (b) polarization hotspots

Table 4. Comparison of energy loss examined by QDE

Work	Total energy loss (meV)	Average energy loss per cycle (meV)
[9]	22.6	2.06
[10]	17.1	1.55
[11]	19.5	1.77
[11]	10.8	0.981
[12]	33.6	3.06
[13]	7.32	0.665
[15]	7.88	0.716
[15]	6.83	0.621
[16]	28.7	2.61
Proposed	5.74	0.522

Table 5. Comparison of cost functions

Work	#MV	#NOT	#CO	Delay (clock-zone)	Area (μm²)	Energy (eV)	ADC	QSC	EDC
[9]	4	2	0	6	0.059	0.08332	2.12	648	0.249
[10]	4	2	0	6	0.056	0.05840	2.01	648	0.122
[11]	4	2	0	5	0.047	0.09859	1.17	450	0.243
[11]	2	1	0	7	0.032	0.04427	1.56	245	0.096
[12]	3	1	0	5	0.047	0.07084	1.17	250	0.125
[13]	2	0	0	6	0.018	0.03822	0.64	144	0.052
[15]	2	0	0	5	0.017	0.04042	0.42	100	0.040
[15]	2	1	0	5	0.018	0.03448	0.45	125	0.029
[16]	4	2	0	8	0.105	0.15232	6.72	1280	1.484
Proposed	2	1	0	5	0.013	0.03334	0.32	125	0.027

#: number of MV: Majority voters, NOT: NOT gate, CO: Crossovers, Energy: QCAPro at γ =1.0 E_K

7 Conclusion

This work introduced a simple and better-performing QTFF with two standard inputs (T and clock) and two standard outputs Q and $\bar{Q}$, like any digital T-flipflop. This work began by conducting a thorough review of existing works related to QTFF and identifying key issues that served as a foundation for this research. Building upon these prior works, a new QTFF layout that combines MVs with a memory loop is presented. This approach enabled us to achieve improved functionality and reduced area overhead compared to previous designs. QCADesigner tool is used to create the layout. To evaluate the performance of the proposed design, an intensive experiment has been conducted using various benchmarks and compared them with existing QTFF designs. As a note, the energy loss has been calculated with two different tools (QCAPro and QDE), indicative of a more precise performance assessment. The experiments result clearly demonstrated the superiority of the proposed design in terms of energy loss, cost, and area utilization. This work has highlighted the potential of QCA technology in delivering efficient and high-performance QCA circuits. It is anticipated that the findings will inspire further advancements in QCA-based flipflop designs, paving the way for the development of more efficient and reliable QCA circuits in the future.

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