Journal of Electrical Engineering, Vol. 74, No. 5, 2023, pp. 390-402

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Realization of a memcapacitance emulator utilizing a singular current-mode active block

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This paper introduces a novel circuit design for a memcapacitance emulator, employing a single Voltage Differencing Current Conveyor (VDCC) as its core element. The emulator circuit has been intricately designed, employing only capacitors as grounded passive components. One remarkable aspect of these circuits is their inherent electronic tunability, allowing for precise control of the achieved inverse memcapacitance. The theoretical analysis of the emulator includes a comprehensive examination of potential non-idealities and parasitic influences. Careful selection of passive circuit elements has been made to minimize the impact of these undesirable effects. In contrast to extant designs cataloged in the existing literature, the presented circuitry manifests remarkable simplicity in its configuration. Furthermore, it exhibits a wide operational frequency range, extending up to 50MHz, and effectively clears the non-volatility criterion. To substantiate the efficacy of the devised circuits, comprehensive LTSpice simulations have been conducted, employing a 0.18 μm TSMC process parameter and a power supply of ±0.9 V. These simulations provide robust evidence of the emulator's performance, reaffirming the feasibility and practicality of the proposed approach in the domain of memcapacitance emulation.

Key words: memcapacitor, emulator, VDCC, grounded passive components, electronic controller, simulation.

1 Introduction

The increasing demand for advanced technological solutions has led researchers to establish more intricate prerequisites in both research and the development of complex systems. These systems require the seamless integration of subsystems characterized by diverse physical attributes. To model nonlinear phenomena occurring across various physical processes, traditional components such as resistors, capacitors, and inductors are commonly employed. These components encapsulate the fundamental correlations between current, electrostatic, and magnetic fields, providing a framework to comprehend reality and adhere to its underlying principles. In 1971, the memristor concept was introduced, expanding the fundamental elements in this realm [1]. Later, in 1980, an array of additional components known as Higher Order Elements (HOEs) were introduced, further enriching the understanding of these systems [2-4]. The memristive concept was subsequently extended to include meminductors and memcapacitors. These entities belong to a subclass of two-terminal devices, where their inductance or capacitance is determined by the internal state of the system. Due to their exceptional attributes, these components find diverse applications across various domains, including analog memory, adaptive filters, relaxation oscillators, neuromorphic circuits, biomedical devices, generators of chaotic signals, low-power computational paradigms, programmable analog circuits, and resistive random-access memory (RRAM), considering that such circuits can store information without the need for a power source, among others [5].

The memcapacitor is defined as

$$v_C(t) = C_M^{-1}(x, q, t)q(t),$$

$$\dot{x} = f(x, q, t) \tag{1}$$

where $q(t)$ is the total charge on the memcapacitor at time t, $v_c(t)$ is the corresponding voltage, and $C_M{}^{-1}(x, q, t)$ is an inverse memcapacitance. The above formula of the memcapacitor can be converted to

$$v_C(t) = C_M^{-1}\left[\int_{t_0}^{t} q(\tau)d\tau\right]q(t) = C_M^{-1}(\sigma)q(t) \tag{2}$$

known as a charge-controlled memcapacitor. Here, σ is the integral of q with respect to time t. Like the meminductor, the memcapacitor is a memory element which retains memory of the past dynamics, providing the connection between flux and time integral of the charge, whereby its capacitor value depends on the history, since the memcapacitor features a nonlinear capacitor change. The memcapacitor gives a pinched hysteresis loop in charge and voltage plain, and can be built in both voltage-controlled and charge-controlled topologies.

Research on memelements, specifically mem-inductors and memcapacitors, has attracted significant

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https://doi.org/10.2478/jee-2023-0047, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

attention in the last two decades due to their unique characteristic of lacking a physical solid structure. The effective development of these components requires emulator circuits capable of faithfully replicating the fundamental attributes of ideal memelements, as defined by established theoretical principles [1-5]. Furthermore, the necessity for compatibility with CMOS technology emphasizes the requirement for these emulator circuits, enabling their practical implementation and validation. To meet the specified requirements, the emulator circuits must exhibit precise control over both AC and DC performance parameters across a wide operational frequency range. Current mode (CM) active blocks have emerged as the preferred foundation for innovative emulator solutions. This preference is based on their inherent advantages, such as reduced power consumption, extensive frequency coverage, and minimal parasitic effects. In contrast, traditional operational amplifiers (OAs) exhibit higher DC power consumption, limited operational frequencies, and increased parasitic effects when compared to CM configurations. Additionally, the incorporation of a multiplier within the circuit introduces complexities and constraints on the achievable operational frequency.

Given the anticipation of a delay in the commercial availability of meminductors and memcapacitors, researchers have focused on developing various SPICE models [6-8] and emulator circuits [9-21] to explore the complexities of these devices' dynamics. To replicate the behaviors of meminductive and memcapacitive elements, investigators have designed mutator circuits capable of transforming memristors into either meminductive or memcapacitive entities [9, 10]. In the realm of memcapacitor emulators, these constructs can be broadly categorized into two groups: grounded [11, 15-17, 19, 20] and floating [9, 10, 12-14, 18, 21]. Grounded memcapacitors involve fewer active and passive components compared to their floating counterparts, although their applications are relatively limited. On the other hand, designing floating memcapacitors is a more complex task. The key feature of floating memcapacitors lies in their electronic tunability, although their performance assessment primarily relies on simulation results. For instance, Vista and Ranjan [12] introduced a floating memcapacitor grounded in a dual X current conveyor differential input transconductance amplifier (DXCCDITA), using a single DXCCDITA and three passive elements. Similarly, other configurations of floating memcapacitors [9, 10, 12] incorporate electronically tunable attributes, with validation predominantly based on simulation results. In a study by Ananda et al. [13], a floating memcapacitor utilizing a varactor diode was presented, comprising four AD844s, one TL084, six resistors, two capacitors, and a singular varactor diode. Sharma et al. [14] proposed a floating charge-controlled memcapacitor, integrating two CCIIs, one multiplier, and three passive components. This memcapacitor circuit was evaluated using both simulation and experimental outcomes, although it lacked electronic tunability. In their previous work [18], Ananda et al. introduced a floating memcapacitor configuration involving two OTAs, one unity gain amplifier (UGA), and two MOS capacitors. In a more recent paper in 2023 [21], Ananda et al. presented an alternate floating memcapacitor circuit incorporating one voltage difference transconductance amplifier (VDTA), one OTA, one buffer, and four passive elements. The upper operational frequencies of these configurations were noted as 1.2 MHz and 24 MHz, respectively. It is worth noting that the count of active and passive components in the aforementioned floating memcapacitors exceeds that of the memcapacitor proposal outlined in this present study, indicating the evolving complexity and diversity in the field of memcapacitor emulation techniques.

This study introduces an innovative approach to create emulators for floating memcapacitors, utilizing a single active block for electronic modulation of their characteristics. This design reduces the impact of existing nonlinearities, enhancing practical performance and resulting in circuits with favorable impedance characteristics. Central to this design is the Charge-Controlled Memcapacitive Emulator (MCE), utilizing the Voltage Differencing Current Conveyor (VDCC). This architecture combines an Operational Transconductance Amplifier (OTA) with a modified current conveyor, a voltage-to-current converter, and two grounded capacitors. This strategic approach capitalizes on the advantages of the second-generation current conveyor (CCII), offering a broad dynamic range, increased linearity, and substantial signal bandwidth while minimizing the need for multiple floating elements typically required in CCII-based configurations. The VDCC configuration allows the realization of circuits in both differential and dual-input modes. It offers the advantage of electronically adjustable transconductance gain while enabling the transmission of voltage across the relevant terminal. To operate within elevated frequency domains, a MOS capacitor is integrated, replacing the conventional capacitor. An essential feature of this design is its elimination of meticulous component or parameter matching requirements. In the envisioned floating memcapacitance mode, the circuit offers a versatile choice between soft and hard switching mechanisms, achievable by manipulating either capacitance values or the frequency of the current excitation signal, without changing any circuit topology. Variations in the operational frequency and amplitude of the input current signal noticeably impact the width of the pinched hysteresis loop. MCE with such mechanism practically exhibit two states: high and low

memcapacitance such as transistors and can therefore be called two terminal transistors (to design MCE that has a smooth switching voltage-charge relationship is easier than designing an MCE that exhibits hard switching behavior). For this reason, a proposed emulator circuit is a good candidate for realization of a memory element instead of several transistors, thanks to their scalability, efficiency, and energy consumption. Emulators exhibiting hard switching behavior, like the one proposed here, find relevance in spiking and bursting neuron circuits, as they demonstrate a binary state: high and low memcapacitance-switches from high capacitive state to low capacitive state suddenly. A noteworthy aspect of this design is its deliberate omission of multiple multipliers, eliminating unnecessary bulkiness and making the proposed circuits more compact and operationally efficient. This streamlined approach not only enhances the practical feasibility of implementing memcapacitor emulators but also contributes to the advancement of electronic circuit design in the domain of memristive systems.

The effectiveness of the proposed emulator has been rigorously validated through comprehensive LTSpice simulations conducted using the 0.18 μm TSMC CMOS technology. These simulations spanned a wide frequency spectrum, reaching up to 50 MHz. The presented emulator boasts several noteworthy advantages, including an extended operational frequency range, electronic adjustability through bias voltage manipulation, utilization of grounded capacitors conducive to monolithic IC fabrication, and a streamlined transistor count. The results obtained from these simulations align seamlessly with the relevant theoretical predictions, providing robust confirmation of the emulator's efficacy. This emulator employs advanced circuitry techniques to replicate the behaviors of floating memcapacitors, essential components in emerging electronic systems. This innovative design sets the stage for promising outcomes, emphasizing precision and control. It paves the way for exploration and practical applications in various fields, including memristor-based neural networks, adaptive filters, and energy storage systems.

2 Proposed configurations

Figure 1 illustrates the proposed configurations of the floating memcapacitor emulator circuit.

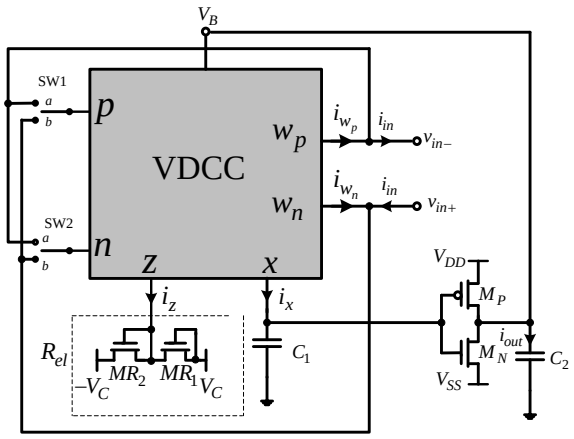


Fig. 1. Floating memcapacitor emulator based on VDCC

The memcapacitive emulator (MCE) architecture incorporates two grounded capacitors, an electronically adjustable resistor (R_{eq}), and a voltage-to-current (*V-I*) converter in its second stage. Figure 1 illustrates the terminal characteristics of the Voltage Differencing Current Conveyor (VDCC), as described in Eqn. (1) through a hybrid matrix formulation.

$$\begin{bmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_{w_p} \\ i_{w_n} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 & 0 \\ 0 & 0 & \gamma & 0 \\ 0 & 0 & 0 & \alpha_p \\ 0 & 0 & 0 & -\alpha_n \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \end{bmatrix} \tag{3}$$

The Voltage Differencing Current Conveyor (VDCC) evinces substantial impedance characteristics across its terminal set, excluding the *x* terminal. Herein, the symbol β denotes the deviation in tracking precision observed within the OTA stage of the VDCC, theoretically attaining an optimal value of 1. Correspondingly, the non-ideal voltage amplification between the *z* and *x* terminals is denoted as γ, with its ideal value being 1. Moreover, α_p and α_n respectively denote the non-ideal current amplification between the *x*, w_p, and w_n terminals, ideally maintaining a value of 1. The transconductance gain of the VDCC can be calculated using the following formula (V_{B1} is the bias voltage (see Fig. 2) and V_{Tn} is the threshold voltage of NMOS transistor):

$$g_m = k\left(V_{B1} - V_{Tn} - V_{SS}\right), \tag{4}$$

where

$$k = B\mu_{nB}C_{oxB}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_{MB1}\left(\frac{W}{L}\right)_{MN}}. \tag{5}$$

Parameter $(W/L)_{MN}$ (W/L is the ratio of the gate width to the gate length of the corresponding MOS transistor) is characterized by the equivalence of $(W/L)_{M1}$ and $(W/L)_{M2}$ and the mirroring of current between transistors M_3, M_4, M_5, and M_6 is represented by the factor denoted as B. Additionally, μ_{nB} signifies the electron mobility, and C_{oxB} denotes the oxide gate capacitance per unit area of the M_{B1} transistor. Upon examining Eqn. (3), it is apparent that terminals p, n, and z serve as transconductance amplifier nodes, while the remaining ports (x, w_p, and w_n), including the output z from the initial stage, as an interface with the internal current conveyor phase. These dual stages are implementable using CMOS technology, as illustrated in Fig. 2, involving a total of 24 MOS transistors in their collective composition.

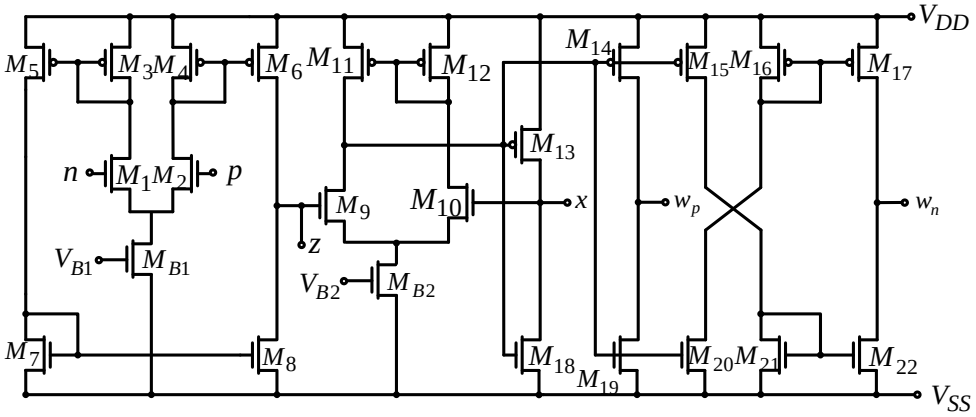


Fig. 2. CMOS implementation of VDCC

The modification of the equivalent resistance R_{el}, achieved through the utilization of two p-MOS transistors shown in Fig. 1, connecting the specified node of the VDCC to the ground reference, can be accomplished by adjusting a control voltage, denoted as V_c. This relationship can be concisely expressed as follows:

$$R_{el} = \frac{1}{2\mu_p C_{ox}\left(V_c - V_{Tp}\right)}\left(\frac{1}{W/L}\right)_{MR} \tag{6}$$

Parameter $(W/L)_{MR}$ is characterized by the equality of $(W/L)_{MR1}$ and $(W/L)_{MR2}$. In high-frequency scenarios, an alternative method involves incorporating MOS capacitances within emulator circuits, replacing the grounded capacitances as shown in Fig. 1. This substitution offers additional advantages in terms of integrated circuit implementation.

Emulating the behavior of a floating memcapacitor is a highly complex task. The compact and innovative design presented in this study is unprecedented in existing literature. By analyzing the configurations depicted in Fig. 1 and exploring the functional relationships among the VDCC's ports, we can draw the following conclusions:

$$i_{W_p} = -i_{W_n} = \alpha_p i_x = i_{in}$$
$$\Rightarrow v_x(t) = \frac{1}{\alpha_p C_1}\int_0^t i_{in}(t)dt = \frac{1}{\alpha_p C_1}q(t)$$

$$i_{out}(t) = g_{m0}v_x(t) \Rightarrow V_B(t) = \frac{1}{C_2}\int_0^t i_{out}(t)dt =$$
$$= \frac{g_{m0}}{\alpha_p C_1 C_2}\int_0^t q(t)dt = \frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t) \tag{7}$$

where $\sigma(t)$ is time integral of charge. It is follows:

$$i_z = \pm\beta g_m(v_{in+} - v_{in-}) =$$
$$= \pm\beta k(V_B(t) - V_{Tn} - V_{SS})(v_{in+} - v_{in-})$$

$$v_z = R_{el}i_z = \frac{v_x}{\gamma} = \frac{1}{\alpha_p\gamma C_1}q(t)$$
$$\Rightarrow \beta k R_{el}(V_B(t) - V_{Tn} - V_{SS})(v_{in+} - v_{in-})$$
$$= \frac{1}{\alpha_p\gamma C_1}q(t) \Rightarrow$$

$$(v_{in+} - v_{in-}) =$$
$$= \pm\frac{1}{\beta k R_{el}\left(\frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t) - V_{Tn} - V_{SS}\right)\alpha_p\gamma C_1}q(t) \tag{8}$$

As a consequence, the resultant memcapacitance equivalence can be formulated as follows:

$$C_M^{-1} = \pm \frac{1}{\beta k R_{el}\left(\frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t) - V_{Tn} - V_{SS}\right)\alpha_p \gamma C_1}. \quad (9)$$

By carefully selecting the appropriate port of the VDCC to which the input voltage of the intended emulation circuit connects – a task accomplished through the precise positioning of switches SW1 and SW2 – the behavior of the memcapacitor response can be determined. This strategic decision determines whether the pinched hysteresis loop follows quadrants 1 and 3 (indicating direct memcapacitance) or quadrants 2 and 4 (indicating inverted memcapacitance, often referred to as negative memcapacitance).

Whether the circuit in Fig. 1 will have a soft or hard switching characteristic, depends on the position of the breakpoints on the pinched hysteresis characteristic, which are determined by the moment when the charge on the proposed emulator circuits reaches the maximum value. These points are determined by the moment when the input current signal reaches the transition point – the so-called zero-crossing (assuming the input current is defined as $I_m \cos \omega t$, and provided that the value of the voltage is as small as possible, i.e. converges to zero. In this way, the transient characteristic of the realized memcapacitance becomes closer to the axis q, and the circuit realizes the hard switching characteristic. The value of the input voltage at the moment when there is a change in the direction of movement of the operating point on the transient characteristic, based on the above assumptions is determined as

$$\begin{aligned} v(t_1) &= \mp \frac{I_m}{\alpha_p \beta \gamma k R_{el}[V_{SS} + V_{Tn}]\omega C_1} \to 0 \\ \frac{\omega \alpha_p \beta \gamma k R_{el} C_1}{I_m}&[V_{SS} + V_{Tn}] >> 1 \end{aligned} \quad (10)$$

Referring to the final relation in Eqn. (8), it is assumed that the maximum charge occurs when the excitation current reaches its peak value and the charge integral approaches zero. By choosing the value of the frequency of the current excitation signal or the size of the capacitor (Eqn. (10)), it is possible to change the behaviour of the proposed emulator circuit-switching characteristics.

On the other hand, by carefully selecting how the input voltage is connected, achieving an inverted memcapacitance profile is possible. Emulator circuits that exhibit hard switching behavior are useful in configurations like spiking and bursting neuron circuits. These circuits demonstrate a dual state, representing high and low memcapacitance. The transition to an inverted operational mode is achieved by establishing a relationship between the input voltage and the accumulated charge. This facilitates an operational mode characterized by incremental changes. In the direct mode, the memcapacitor emulator operates with decreasing values. Conversely, in the incremental mode, the memcapacitance value starts from an initial negative magnitude, as described in Eqn. (9).

3 Non-ideal and parasitic analysis

In real-world situations, the Voltage Differencing Current Conveyor (VDCC) often demonstrates non-ideal gains, referred to as tracking errors, as discussed earlier in this paper. These deviations in tracking accuracy remain consistent and are not influenced by changes in frequency, ranging from low to medium frequencies. Upon examining the relationships outlined in Eqn. (9), it is evident that the proposed configurations exhibit sensitivities, where both passive and active sensitivities are either equal to or less than unity in magnitude. Based on this observation, we can conclude that the designed circuits have minimal passive and active sensitivities.

Considering the terminals p, n, z, w_p, and w_n, a set of parasitic resistances (R_p, R_n, R_z, R_{wp} and R_{wn}) along with parasitic capacitances (C_p, C_n, C_z, C_{wp} and C_{wn}) collectively influence the system. In the ideal VDCC scenario, these parasitic resistances tend toward infinity, while the parasitic capacitances become negligible. Additionally, at the x port, a parasitic resistance R_x and an associated parasitic inductance L_x are in series configuration, with values approximating zero in an ideal VDCC context. Considering these parasitic components, the equivalent memcapacitance for the emulator circuits depicted in Fig. 1 can be expressed as follows:

$$C_M^{-1} = \pm \frac{1 + sR_{el}C_z}{\beta k R_{el}\left(\frac{g_{m0}}{\alpha_p C_1 (C_2 + C_{V-I}) C_2}\sigma(t) - V_{Tn} - V_{SS}\right)\alpha_p \gamma C_1} \quad (11)$$

Based on the relationship presented in Eqn. (11), the careful selection of external capacitors C_1 and C_2 is crucial. Their values need to significantly exceed the magnitudes of the parasitic capacitances associated with their respective ports. This intentional choice ensures the effective reduction of adverse effects caused by parasitic capacitances across various operational frequencies. Simultaneously, to mitigate the impact of parasitic resistances, values for C_1 and C_2 must be chosen so that their combined impedance remains significantly lower than the inherent parasitic resistances of the VDCC ports.

It is important to note that the transconductance demonstrated by the Operational Transconductance Amplifier (OTA) cell within the VDCC configuration is influenced by frequency. Its bandwidth restriction is well-represented by a single-pole model. Therefore, the characterization of the transconductance gain and the

parameter k for the initial stage of the VDCC can be expressed as follows:

$$g_m = g_{m_0}\frac{\omega_g}{(s+\omega_g)},\ \ k = k_0\frac{\omega_k}{(s+\omega_k)} \qquad (12)$$

In the provided equations, the transconductance gain is denoted as g_{m0}, and the amplification factor of the OTA cell at zero frequency is represented as k_0. The pole frequencies, $\omega_g=1/\tau_g$ and $\omega_k=1/\tau_k$ correspond to the delays τ_g and τ_k. respectively. These pole frequencies establish the boundaries defining the system's bandwidth limitations. By substituting the values of g_m and k into Eqn. (11), a deeper understanding of the frequency characteristics of the emulators can be gained, taking into account their dependence on non-ideal factors. The emulators illustrated in Fig. 1 operate within a specific operational frequency range characterized by $\omega<<\min(\omega_g, \omega_k)$. The exact values of these pole frequencies in Eqn. (12) depend on the practical implementation of the VDCC. To enhance the bandwidth of the VDCC, introducing a compensatory resistor R at the p port can be a viable strategy. This modification alters the transconductance gain, resulting in a new value expressed as $g_m=g_{m0}/(1+g_{m0}R)$. Consequently, the bandwidth of the OTA cell can be adjusted accordingly.

4 Simulation results

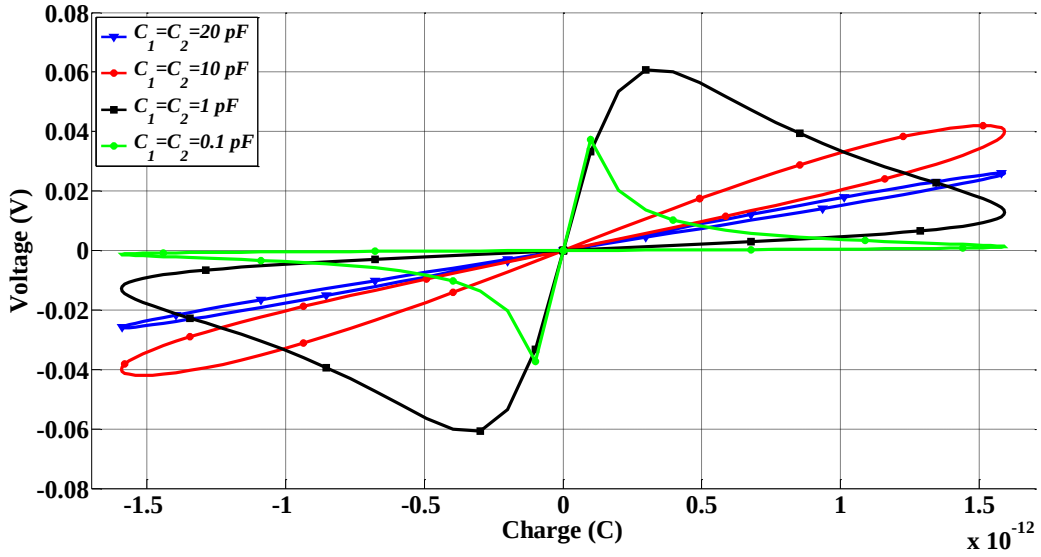
The proposed MCE circuits underwent comprehensive simulations using LTSpice software, employing TSMC CMOS 0.18 μm process model parameters. In the specific MCE arrangement based on the VDCC, the V_{B2} voltage was set at 0 V. In this configuration, the bulk terminals of pMOS and nMOS transistors were connected to their corresponding source terminals and anchored at the most negative voltage point (V_{SS}). The dimensions of the VDCC transistors (as detailed in Tab. 1 and Fig. 2) were specified as follows: M_{B1}, M_{B2}, MR_1, and MR_2 had dimensions of 3.6 μm/1.8 μm, 3.06 μm/0.72 μm, 60 μm/2 μm, and 60 μm/2 μm, respectively. To ensure the saturation state of M_N and M_P and effective V-to-I conversion, the DC supply voltages were set at ±0.9 V. An electronic resistor, formed by only two PMOS transistors, was adjustable through control voltage manipulation. Using a control voltage of 0.65 V resulted in an equivalent resistance magnitude of R_{el}=1.47 kΩ. Calculations indicated the power consumption of the proposed VDCC (Fig. 2) to be 0.869 mW.

Table 1. Dimensions of the transistors – VDCC

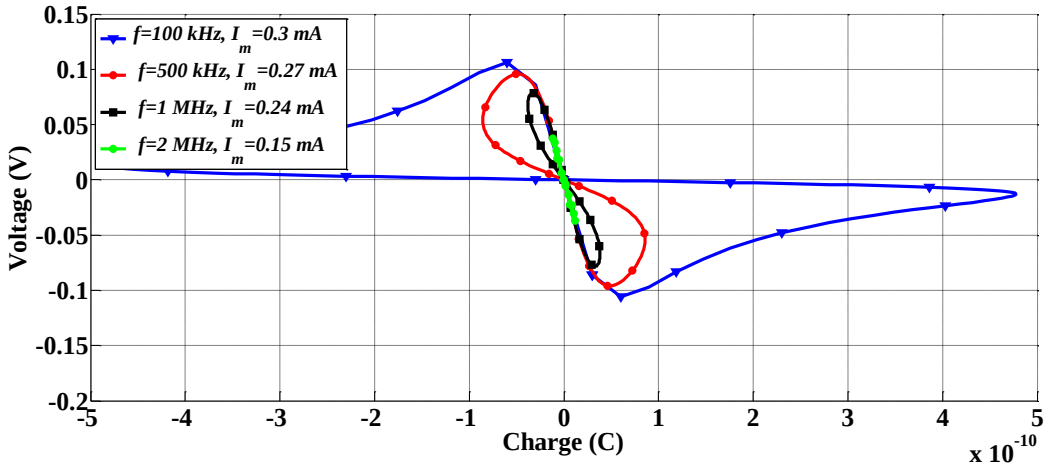
Transistor	W (μm)	L (μm)
M_1-M_4	3.6	1.8
M_5, M_6	7.2	1.8
M_7, M_8	2.4	1.8
M_9, M_{10}	3.06	0.72
M_{11}, M_{12},	9	0.72
M_{13}-M_{17}	14.4	0.72
M_{18}-M_{22}	0.72	0.72
M_P	13	0.36
M_N	4	0.36

During the simulation analysis of the Memcapacitive Emulator (MCE), a sinusoidal current signal characterized by varying frequencies was employed. The input sinusoidal current signal exhibited an amplitude of I_m=100 μA. Figure 3(a) illustrates the outcomes of the MCE simulation, conducted at an excitation current signal frequency of 10 MHz, with a consideration of diverse ground capacitance values for C_1 and C_2. This analysis explores the transition between different switching modes. When the proximity of capacitance reduces, the inflection point on the transient characteristic approaches the q-axis, causing the voltage magnitude at that point to approach zero. This aligns with theoretical predictions. Practically, changes in capacitor values, whether increased or decreased, result in an inversely proportional alteration in the area enclosed within the pinched hysteresis curve. This behavior is due to the dominance of the linear time-variant aspect over the linear time-invariant facet of the memcapacitor, as described in Eqn. (9). A similar effect can be achieved by adjusting the frequency of the input current signal.

Consistent with theoretical predictions, the MCE operates in an inverting mode. To validate this mode, performance evaluations were conducted at various excitation signal frequencies and amplitudes while maintaining a constant capacitance configuration (C_1=C_2=100 pF) as depicted in Fig. 3(b). Simulation results indicate that as the operational frequency increases, the spatial coverage of the lobes within the q-v plane decreases. Moreover, as the operational frequency rises, the area enclosed by the pinched hysteresis curve contracts, making the memcapacitor behavior more akin to that of a conventional capacitor. This transformation is due to the diminishing role of the variable component specified by Eqn. (9).



(a)



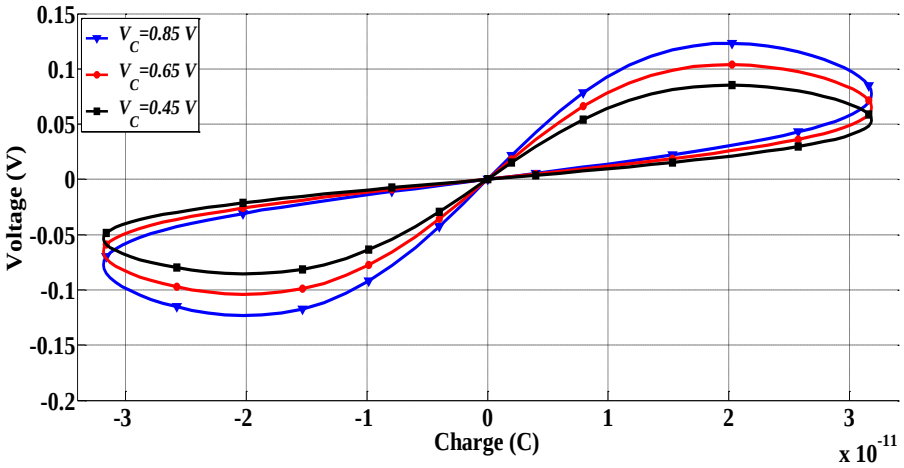
(b)

Fig. 3. Transient behaviors exhibited by the presented emulator circuit are illustrated as follows: (a) encompassing various capacitance values, specifically at a frequency of f=10 MHz, and (b) spanning distinct frequencies and amplitudes of the input current signal within the inverting mode of operation, with C_1=C_2=100 pF.

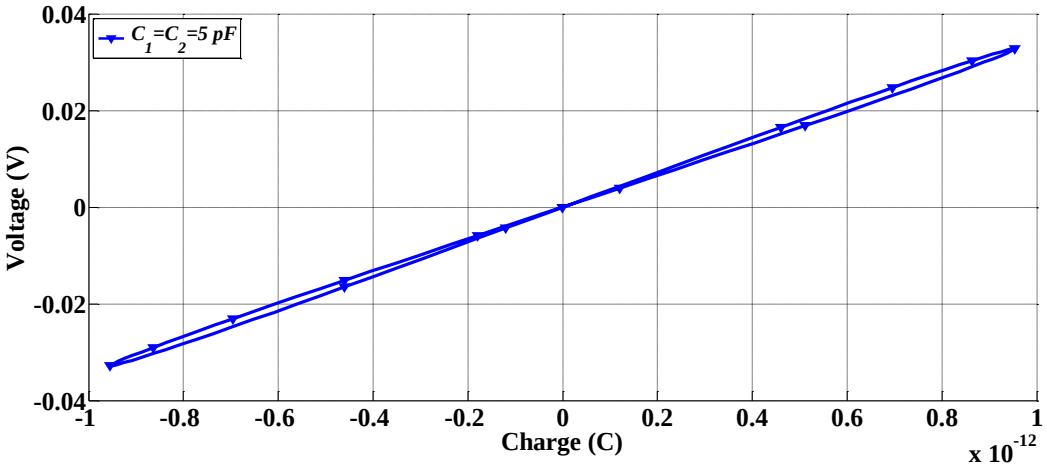
A distinctive feature of the proposed MCE is its electronically adjustable nature: the control voltage V_c can be flexibly modified to regulate the charge within the circuit. Figure 4(a) illustrates the input charge-voltage relationships displayed by the developed memcapacitor emulator across various V_c values, with C_1=C_2=50 pF, f=1 MHz, and I_m=0.2 mA. In Fig. 4(b), the peak operational frequency for the circuit is limited to 50 MHz due to practical constraints related to achievable capacitance values within the integrated approach. These capacitance values, especially those of C_1 and C_2, inevitably approach equivalence with the parasitic capacitances inherent to the VDCC ports.

To analyze the transient behaviors of the proposed memcapacitor emulators, simulations were conducted using sinusoidal input current signals with a frequency of 10 kHz and an amplitude of 100 μA, as depicted in Fig. 5. Figure 5(a) accurately presents the simulation results, where the generated voltage signal notably deviates from the sinusoidal waveform. This deviation arises due to the inherent time-varying nature of memcapacitance. Increasing the frequency of the input current signal results in a corresponding reduction in the phase difference between the input voltage signal and the associated charge value of the memcapacitance. The thermal performance of the circuits in Fig. 1 was systematically examined through simulations conducted across three different temperature scenarios, as illustrated in Fig. 5(b). This empirical investigation confirms that these circuits exhibit the expected

attributes over a wide range of temperatures. Specifically, the configurations with C_1=C_2=50 pF, f=1 MHz, and I_m=0.25 mA were the focal parameters. It is important to note that as the temperature decreases, there is a proportional increase in the current flow within the memcapacitor components.

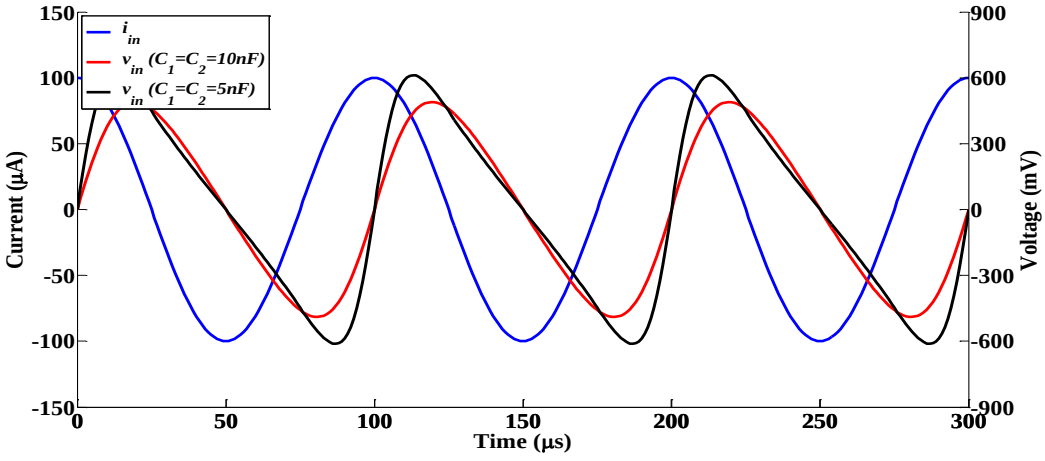


(a)

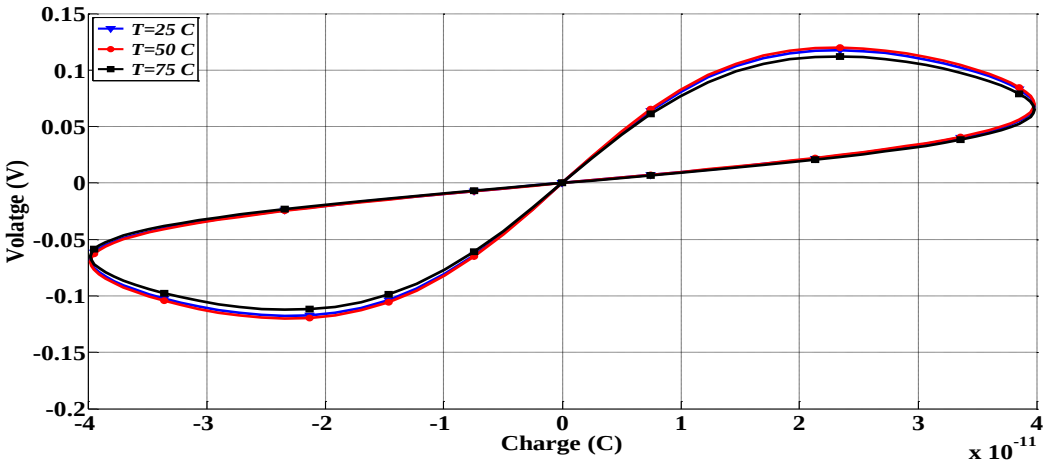


(b)

Fig. 4. (a) The input voltage-charge relationships for proposed MCE for the different control voltage V_C, (b) transient response of proposed MCE for frequency of 50 MHz and amplitude I_m=300 μA.



(a)



(b)

Fig. 5. (a) Time responses-time-domain response of the proposed MCE (b) hysteresis loop at various temperatures in MCE.

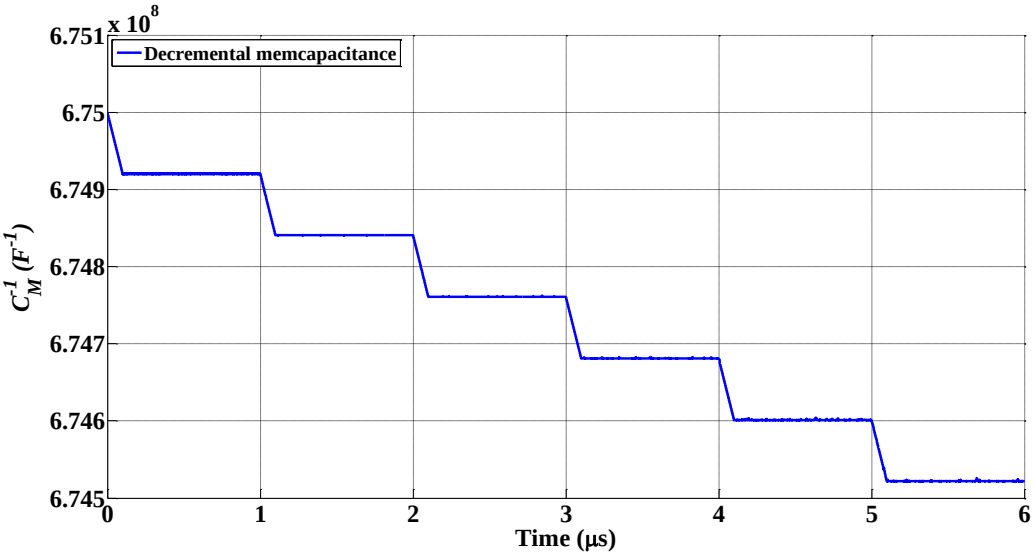


Fig. 6. Variation of memcapacitance with time for proposed MCE

Furthermore, our investigation delves into the inherent non-volatile characteristics of the mem-system, focusing keenly on a critical aspect of the Memcapacitive Emulator (MCE). In the context of the proposed MCE, we conducted a detailed inquiry involving a pulse input characterized by an amplitude of 0.5 mA, a periodic interval of 1μs, and a pulse width of 0.1 μs. Simultaneously, external capacitance parameters were meticulously set to C_1=C_2=1 nF. The simulation results, vividly presented in Fig. 6, unequivocally confirm the constancy of memcapacitance magnitude even in the absence of a pulse signal. This noteworthy observation emphasizes the robust memory traits embedded within the circuit, particularly during the temporal gaps between pulses. These specific configurations provide a practical framework for investigating and formulating neuromorphic circuits incorporating synaptic plasticity, with a specific focus on long-term potentiation (LTP). In the realm of neuroscience, LTP signifies the enduring strengthening of synapses based on recent activity patterns, constituting a foundational mechanism governing learning and memory processes [22]. Moreover, by strategically transitioning the proposed MCE circuit into the inverting mode, an incremental operational mode can be effectively achieved. In this operational context, the memcapacitance value ascends from its initial negative datum, a phenomenon elucidated cogently by Eqn. (9).

4.1 Process variation

Figure 7 conducts a comprehensive exploration of distinct process corners, encompassing Nominal NMOS Nominal PMOS (NN), Fast NMOS Fast PMOS (FF),

Slow NMOS Slow PMOS (SS), Fast NMOS Slow PMOS (FS), and Slow NMOS Fast PMOS (SF) variations. This meticulous scrutiny holds paramount significance in the context of monolithic integration efforts. The empirical evaluation of the proposed configurations involves practical testing through parameter modulation within the simulation process. This extensive endeavor requires precise adjustments to the dimensions of the MOS transistors in use, considering their observable effects on the parameters stored in the LTspice library. However, it is important to note that this variation may potentially lead to over- or underestimation of specific parasitic capacitances.

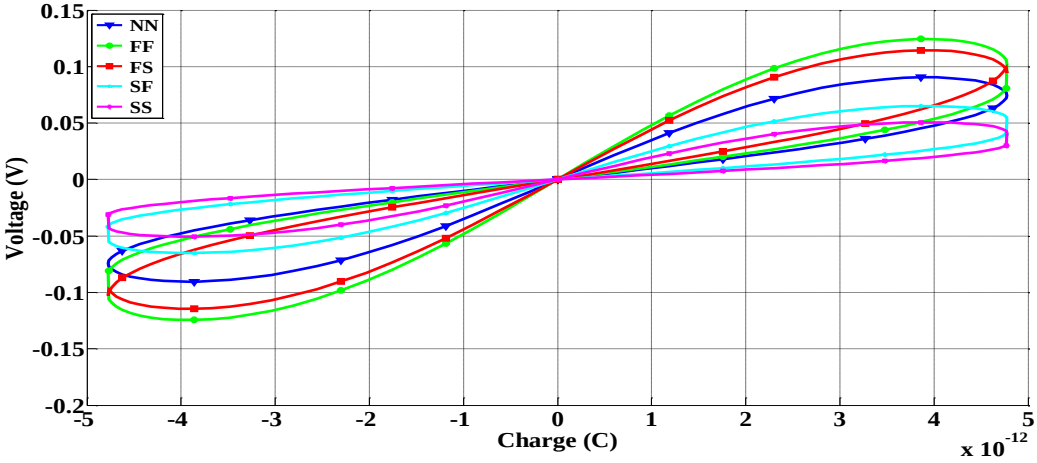


Fig. 7. Pinched hysteresis loop variation at different process corners

In this study, a crucial aspect of our focus on the proposed MCE is the meticulous analysis of process corners, conducted at a frequency of 10M Hz, with C_1=C_2=10 pF and I_m=0.3 mA, as clearly outlined in Fig. 7. Results from this analysis reveal, as expected, that the current flow in the FF mode surpasses that in the SS mode. Despite noticeable variations in the hysteresis loop area, all configurations of the proposed memcapacitance circuits consistently exhibit a pinched hysteresis loop, a significant characteristic across all process corners. Additionally, the absence of offsets in the characteristics enhances the robustness of the circuitry. It is important to note that any potential offsets in practical applications can be effectively mitigated through appropriate compensation techniques. The simulation outcomes unequivocally confirm that the FF mode demonstrates a higher current flow compared to the SS mode, aligning with our initial expectations. This asymmetry results in a subdued current flow within the SS process corner, contrasting with its FF process corner counterpart. In summary, our findings conclusively demonstrate that the proposed circuitry adeptly navigates a wide range of temperature variations and diverse process corner conditions, highlighting its versatility and robustness across these distinct operational scenarios.

4.2 Comparison

Table 2 offers a detailed comparison between previously documented memcapacitor emulators and our innovative Memcapacitive Emulator (MCE). This analysis focuses on design and performance aspects, highlighting recent advancements in the field. Various criteria, such as active and passive components, tunability, frequency range, mode of operation, and power supply, are compared. The results clearly show the superiority of our proposed emulator circuits.

Notably, our circuits achieve the highest operational frequency in existing literature while maintaining low power consumption. Their unique ability to manipulate pinched hysteresis loops makes them attractive for applications requiring intelligent parameter modulation to reconcile disparities. These emulators stand out for their streamlined design, wide bandwidth, and seamless integration potential in real-world integrated circuit deployments.

Table 2. Comparison of the exiting MCE with the proposed

Ref.	Number of active comp.	Number of passive elements	Power supply	Maximum operating frequency	Type of emulator (F/G)	Electron. tunability	Need of external memristor
[12]	1 DXCCDITA	1 R, 2 C	±1.25 V	1 MHz	F	No	No
[13]	4 CFOA, 1 OA, 1 VD	5 R, 2 C	±15 V	10 kHz	F	No	No
[14]	2 CCII, 1 AM	4 R, 2 C	±10 V	25 kHz	F/G	No	No
[15]	2 VDCC	2 R, 2 C	±0.9 V	10 kHz	G	Yes	Yes
[16]	2 CCII, 1 AM	2 R, 2 C	±10 V	2 kHz	G	Yes	No
[17]	2 VDTA	2 C	±0.9 V	500 Hz	G	Yes	Yes
[18]	2 OTA, 1 UGA, 2 MOS capacitors	1 R	±15 V	24 MHz	F	Yes	No
[19]	1 VDTA	2 C	±0.9 V	50 MHz	G	Yes	No
[20]	1 FDCCII, 1 AM, 2 MOSFETs	3 C	±0.9 V	1 MHz	G	No	No
[21]	1 VDTA, 1 OTA, 1 Buffer	1 R, 3 C	±0.9 V	1.2 MHz	F	Yes	No
This work	1 VDCC, 2MOSFETs	2C	±0.9 V	50 MHz	F	Yes	No

F=floating
G=grounded
AM=analogue multiplier
VD=varactor diode

5 Conclusion

This paper introduces a new memcapacitance emulator that operates in the current-mode domain, utilizing the Voltage Differencing Current Conveyor (VDCC) architecture. The proposed architectures combine simplicity with versatility, offering tunability through a control voltage and an extended operational frequency range of up to 50 MHz. These configurations achieve superior performance with fewer active elements and grounded passive components compared to existing alternatives, facilitating easy integration with other circuits and expanding the potential applications of mem-systems. The study thoroughly investigates the inherent non-idealities of the VDCC, such as transfer gain discrepancies and the influence of parasitic elements, to understand their impact on memelement emulation. Valuable insights are provided for selecting optimal passive circuit elements. The theoretical foundations are rigorously validated through comprehensive simulation experiments, confirming the emulator's effective operation at frequencies up to 50 MHz under various parameter variations (process, capacitor, temperature, and frequency domains). The proposed memcapacitance emulator features dual switching mechanisms (soft and hard) based on capacitance values or input current signal frequency. The paper outlines the criteria governing the seamless transition between these operational modes. Moreover, the circuit can emulate negative memcapacitance, enabling applications in nonlinear chaos oscillators and neuromorphic computing paradigms. A comparative

analysis with existing solutions unequivocally demonstrates the superiority of the proposed memelement emulator. Significant improvements in power consumption, maximum operational frequency, and the count of essential active components position these circuits as superior alternatives for integrated implementations. This innovative approach overcomes limitations observed in previous implementations, markedly enhancing the efficiency and versatility of the proposed configurations.

Acknowledgment

This research was supported by the Ministry of Education, Science and Technological Development of the Republic of Serbia, and these results are parts of the Grant No. 451-03-47/2023-01/200132 with University of Kragujevac - Faculty of Technical Sciences Čačak.

References

[1] L.O. Chua, "Memristor – The missing circuit element", *IEEE Trans Circ Theory*, vol. 18, pp. 507-519, 1971.

[2] L.O. Chua, "Device modeling via nonlinear circuit elements", *IEEE Trans Circ Syst*, vol. 27, pp. 1014-1044, 1980.

[3] L.O. Chua and S.M. Kang, "Memristive Devices and Systems", *Proc IEEE*, vol. 64, pp. 209-223, 1976.

[4 M. Di Ventra, Y.V. Pershin and L.O. Chua, "Circuit Elements with Memory: Memristors, Memcapacitors, and Meminductors", *Proc IEEE*, vol. 97, pp. 1717-1724, 2009.

[5] N.A. Khalil, F. E. Fouda, L.A. Said, A.G. Radwan, and A.M. Soliman, "A general emulator for fractional-order memristive elements with multiple pinched points and application", *AEU - International Journal of Electronics and Communications*, vol. 124, no. 153338, doi:10.1016/j.aeue.2020.153338, 2020.

[6] D. Biolek, Z. Biolek and V. Biolkova, "SPICE modeling of memristive, memcapacitative and meminductive systems", *In: 2009 European Conference on Circuit Theory and Design. IEEE*, pp.249-252, 2009.

[7] D. Biolek, Z. Biolek and V. Biolková, "Behavioral modeling of memcapacitor", *Radioengineering*, vol. 20, no. 1, pp. 228-233, 2011.

[8] D. Biolek, Z. Biolek and V. Biolková, "PSPICE modeling of meminductor", *Analog Integrated Circuits and Signal Processing*, vol. 66, no. 1, pp. 129-137, 2011.

[9] Z.G. Çam Taşkıran, M. Sağbaş, U.E. Ayten and H. Sedef, "A new universal mutator circuit for memcapacitor and meminductor elements", *AEU - International Journal of Electronics and Communications*, vol. 119, no. 153180, doi: 10.1016/j.aeue.2020.153180, 2020.

[10] A. Singh and S.K. Rai, "VDCC-Based Mem-capacitor/Meminductor Emulator and Its Application in Adaptive Learning Circuit", *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, vol. 45, no. 4, pp. 1151-1163, 2021.

[11] N. Raj, R.K. Ranjan, F. Khateb and M. Kumngern, "Mem-Elements Emulator Design with Experimental Validation and its Application", *IEEE Access*, vol. 9, pp. 69860-69875, 2021.

[12] J. Vista and A. Ranjan, "Simple charge controlled floating memcapacitor emulator using DXCCDITA", *Analog Integrated Circuits and Signal Processing*, vol. 104, no. 1, pp. 37-46, 2020.

[13] D. Yu, X. Zhao, T. Sun, H.H.C. Iu and T. Fernando, "A Simple Floating Mutator for Emulating Memristor, Memcapacitor, and Meminductor", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1334-1338, 2020.

[14] P.K. Sharma, R.K. Ranjan, F. Khateb and M. Kumngern, "Charged Controlled Mem-Element Emulator and Its Application in a Chaotic System", *IEEE Access*, vol. 8, pp. 171397-171407, 2020.

[15] M. Konal, F. Kacar and Y. Babacan, "Electronically controllable memcapacitor emulator employing VDCCs", *AEU - International Journal of Electronics and Communications*, vol. 140, no.153932, soi: 10.1016/j.aeue.2021.153932, 2021.

[16] A. Yesil and Y. Babacan, "Electronically Controllable Memcapacitor Circuit with Experimental Results", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1443-1447, 2021.

[17] M.Z. Hosbas, F. Kaçar and A. Yesil, "Mem-capacitor emulator using VDTA-memristor", *Analog Integrated Circuits and Signal Processing*, vol. 110, no. 2, pp. 361-370, 2022.

[18] Y.R. Ananda, G.S. Satyanarayan and G. Trivedi, "An Optimized MOS-Based High Frequency Charge Controlled Memcapacitor Emulator", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 4, pp. 793-803, 2022.

[19] P.B. Petrovic, "Electronically adjustable grounded memcapacitor emulator based on single active component with variable switching mechanism", *Electronics*, vol. 11, no. 1, pp. 1-15, 2022.
[20] M.O. Korkmaz and A. Yesil, "FDCCII Based New Memcapacitor Emulator Circuit with Electronically Tunable", *Mühendislik Bilimleri ve Araştırmaları Dergisi*, vol. 5, no. 1, pp. 127-134, 2023.
[21] Y.R. Ananda, G.S. Satyanarayan and G. Trivedi, "A High Frequency MOS-Based Floating Charge Controlled Memcapacitor Emulator", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 1189-1193, 2023.
[22] S.F. Cooke and T.V.P. Bliss, "Plasticity in the human central nervous system", *Brain*, vol. 129, pp. 1659-1673, 2006.

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Received 20 August 2023