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Area and power efficient divide-by-32/33 dual-modulus pre-scaler using split-path TSPC with AVLS for frequency divider

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Pre-scalers are electronic circuits used in phase-locked loops to multiply frequencies. This is achieved by dividing the high-frequency signals generated from a voltage-controlled oscillator. The high-frequency operation of pre-scaler circuits leads to significantly higher power consumption. To address this, D flip-flops (D-FF) realized using true-single phase clocking (TSPC) logic. The work suggests incorporating the Adaptive Voltage Level Source (AVLS) circuit with the Dual Modulus Pre-Scaler (DMPS) circuit to reduce power consumption. In addition to the incorporation of the AVLS circuit, pass transistor logic (PTL) used in the feedback, further minimizes transistors and power. This paper proposes three different designs for divide-by-32/33 DMPS circuit. The proposed-1 design combines regular TSPC-based D-FF with PTL in the feedback and an AVLS circuit, resulting in an average power reduction of 36.5%. The proposed-2 design employs split-path TSPC-based D-FF with logic gates and an AVLS circuit, achieving a power reduction of 46.9%. The proposed-3 design employs split-path TSPC-based D-FF with PTL in the feedback and an AVLS circuit, achieving a significant power reduction of 47.8% compared to the existing DMPS circuit and transistor count by 9.1%. The proposed circuits are realized using a CMOS 180 nm technology node. Cadence Virtuoso and Spectre tools are used. The proposed divide-by-32/33 DMPS circuits also realized in the CMOS 45 nm technology node to verify the functionality in the lower technology node. A power reduction of 46.86% observed when compared to the reference circuit. The proposed designs are both power- and area-efficient, making them promising solutions for minimizing power consumption in pre-scaler circuits.

Keywords: AVLS, CMOS, DMPS, Split-path TSPC, TSPC

1 Introduction

Phase-locked loops (PLL) widely used in electronic systems, for synchronization, clock recovery, demodulation, noise, and jitter reduction, and most importantly to perform frequency synthesis in communication systems. PLLs generate an output frequency that is a multiple of the input frequency and maintains the same phase in both input and output signals. PLL comprises a phase detector (phase frequency detector), loop filters, voltage-controlled oscillators (VCO), and frequency dividers. It is essential to design a PLL that consumes less power as it operates at higher frequencies and occupies less area. A simple frequency divider (divide-by-N counter) divides the input signal frequency by N, whereas a dual-modulus pre-scaler (DMPS) divides the input signal frequency by N/N+1 ($N = 2^n$) [1]. Pre-scalers comprise of sequential elements such as flip-flops (FF) and logic gates. The pre-scalers operate at very high frequencies (as VCO generates high-frequency signals) thereby it is necessary to lower the power consumption of DMPS, which can be achieved by reducing the power consumption of the D-FFs and logic gates.

The D-FF realized using pass transistors and basic gates requires more area when compared to other implementations such as TSPC [2, 3], E-TSPC, and split-path/output TSPC implementations. There are several ways to construct a D flip-flop (D-FF), which include using basic gates, pass transistors, transmission gates as well as TSPC [6] and extended-TSPC logic [7]. TSPC logic is preferable compared to other techniques for realizing D-FF in terms of area and power consumption. TSPC logic reduces power at higher frequencies and requires fewer transistors for realization over the conventional implementations. A single-phase non-inverted clock used in TSPC-based D-FF [3] and reduces the delay overhead associated with latches by integrating logic functionality into them. The split-path TSPC-based D-FF can be used in place of regular TSPC as split-output requires only 10 transistors whereas later requires 11 transistors. Pass-transistor logic frequently used as a substitute for CMOS logic to reduce transistor count.

In high-frequency applications, because of higher switching operations/ computations, power dissipation will be more (power dissipation is proportional

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to frequency), so there is a need to reduce power consumption at high-frequency operations. Low-power techniques embedded into the design to achieve power reduction. Adaptive Voltage Level (AVL), clock gating, adiabatic, stack, and sleep transistors are some of the low-power techniques available. AVL is a low-power method to reduce leakage power [6]. Adaptive Voltage Level Source (AVLS) and Adaptive Voltage Level Ground (AVLG) are categories of AVL [8]. The transistors in the AVLS circuit are controlled by this control signal, which is usually a clock signal. The voltage supplied to the pre-scaler is provided by the output of the AVLS circuit, the circuit consume less power when the AVLS circuit is incorporated.

The objective of the work is to design a divide-by-32/33 dual modulus pre-scaler (DMPS) circuit that uses fewer transistors and consumes less power when compared to existing architectures. The proposed divide-by-32/33 DMPS uses split-path TSPC (instead of regular TSPC) logic to realize D-FF, incorporates an AVLS circuit to reduce power and uses pass transistor logic (PTL) to reduce area/transistor count in the feedback of DMPS. The circuits are realized using Cadence Virtuoso in CMOS 180 nm and 45 nm technology nodes, and the simulation is performed on Cadence Spectre. A divide-by-32/33 pre-scaler that consumes minimal power and requires less area is presented.

The paper is categorized into various sections. Section 2 discusses the literature review. The AVLS technique and circuit implementations are elucidated in Section 3. In Section 4, the simulation results are analyzed, and the proposed pre-scalers compared with the present pre-scaler in terms of power consumption. Section 5 summarizes the work and outlines its future scope.

2 Literature review

A pre-scaler is a crucial element (block) in the context of frequency dividers. Pre-scalers operate on high-frequency input signals, which results in higher power consumption.

A TSPC latch with five transistors, six transistors, eleven transistors, a divide-by-2/3 pre-scaler, and a divide-by-2 counter was developed, and their performance was studied in terms of power and delay [1]. First, the area and power of a 2/3 pre-scaler are analyzed. AVLS circuit is included along with a TSPC-based circuit to reduce power. The AVLS-TSPC-based 2/3 DMPS was tested in both divide-by-2 and divide-by-3 modes of operation, with a 1.8 V supply voltage. The 2/3 pre-scalers in [2] are better in terms of area and power consumption when compared to earlier pre-scalers. Pass transistor logic was used to reduce the area of the design and further optimize the power. A TSPC-based 2/3 pre-scaler with low power consumption was designed using three transistors in place of the CMOS logic.

The design of flip-flops affects the performance and power efficiency of digital systems. The performance of a TSPC-based D-FF is better in terms of power and area over a master-slave-based D-FF. Transistor sizes are optimized in the design as per the power delay product (PDP) in [3]. Utilizing 130-nm CMOS process technology, the performance levels of FF designs and their timing characteristics were examined. According to the simulation outcomes, the TSPC-based D-FF performed exceptionally well in terms of PDP, power usage, clock-to-Q latency, and data-to-Q delay, among other performance indices [3]. A low-power single-phase divider for Bluetooth and WLAN presented using CMOS 180 nm technology. The 32/33/47/48 pre-scaler and an enhanced swallow (S) counter constitute the multiband divider [4].

A low-power D-Flip flop circuit employing the AVL approach proposed in [6]. The TSPC divider frequently implemented in pre-scalers. Flip-flops and logic gates are components of a DMPS. TSPC and differential-type flip-flops are used to implement the pre-scaler for division by 2/3. By combining several 2/3 pre-scaler and flip-flop configurations, a 32/33 pre-scaler implemented. A multi-modulus 32/33 pre-scaler operating up to 6.2 GHz is proposed. The proposed divider uses an improved S-counter and consumes less power [9]. Overall power dissipation is decreased by using AVLG technology, which raises the ground potential, and AVLS technology, which lowers the supply potential. Lowering a D-FF's power consumption was the key objective. The device power consumption significantly reduced using the AVLS technique [8]. System-based low-power techniques include adiabatic logic, which requires a minimum of twice the area, despite reducing power. It is used in applications where the power is critical and there is no impediment to a total area [11].

TSPC-based FF based on dynamic FF that executes flip-flop operations at high speed and low power [13]. A clear comparison of the TSPC-based FF designs that are currently used is included in [15]. TSPC-based D-FF can be utilized in applications ranging from digital VLSI clocking systems to buffers, microprocessors, etc. One of the components of wireless communication applications is a frequency synthesizer. A circuit used in high-frequency synthesizer designs is a pre-scaler. The speed of the voltage-controlled oscillator and pre-scaler determines the frequency synthesizer's speed. Flip-flops that are appropriate for high-frequency operations must

be chosen. TSPC flip-flops are used to implement the divide-by-2/3 pre-scaler. By combining 2/3 pre-scaler and flip-flop combinations, the divide-by-32/33 pre-scaler implemented in [17]. Some methods for reducing power consumption include gated leakage transistors (GALEOR), leakage control transistors (LECTOR), AVL, adiabatic logic, stack, and clock gating [18]. Power consumption while operating at higher frequencies requires power reduction techniques, one method involves dividing the VCO output used in the feedback path followed by circuitry that performs the division [20].

The split-output TSPC reduces clock load and hence, possible to minimize the number of clocked transistors with the use of split outputs after the first stage of TSPC-based D-FF [21]. Pre-scalers are used to construct wide-band frequency synthesizers, and when designed employing split-output TSPC-based D-FF in comparison with other D-FF designs, they use less area and power. The split-path TSPC-based D-FF can used in place of regular TSPC as split-path requires only 10 transistors whereas later requires 11 transistors. TSPC logic, PTL, and AVLS approaches can be implemented to minimize power dissipation.

3 Design and implementation of DMPS circuits

DMPS circuits operate at higher frequencies and dissipate more power. To minimize the power consumption of DMPS, low-power approaches need to be included. Low-power techniques can be adapted at a circuit level such as AVLS and AVLG, as well as at the system level using adiabatic logic. According to the literature review, there are numerous methods for reducing power consumption; the AVL technique reduces power with minimal increase in area. This section provides information regarding the design and implementation of the divide-by-32/33 pre-scaler components.

A. Implementation of TSPC-based D-FF

Fundamental elements of sequential digital electronics systems are flip-flops and they are the basic storage elements. DMPS circuits comprise a serial connection of D-FFs and a feedback logic, which produces the required division. Realization of D-FF using TSPC-based logic is preferred because of its low area and low power consumption [2]. A TSPC-based D-FF requires only eleven transistors, realized in stages as shown in Fig. 1. The 11T TSPC-based D-FF uses five p-MOS and six n-MOS transistors. The first stage functions as a transparent latch to receive the input signal when the clock is at logic low, while the second stage's output node is being pre-charged. The third and fourth stages of this cycle only maintain the prior output state. The first stage stops being transparent, and the second stage begins evaluating when the clock changes from low to high. The third stage also turns transparent; sampled values are sent to the output. The last stage of D-FF (the inverter) used to obtain the non-inverted output. The AVLS circuit incorporated into TSPC-based D-FF further minimize supply node potential. Thus, TSPC-based D-FF with an AVLS circuit reduces power with a marginal increase in the transistor count.

According to Table 1, transmission gate-based D-FF implementation requires more transistors than TSPC-based D-FF. Using TSPC logic to realize D-FF eliminates skew issues and take less area and power compared to other variants of D-FF. Split-path/output TSPC is a different variant of TSPC that uses one transistor less to implement D-FF than regular TSPC as shown in Fig. 2. The working of the split-output TSPC circuit is similar to that of regular TSPC circuit. Using split-output TSPC-based D-FF instead of regular TSPC reduces the transistor count by one in D-FF realization [21].

Table 1. Area comparison of D flip-flop circuits

D flip-flop circuits	Transistor count
Transmission gate-based D-FF [3]	18
TSPC-based D-FF [2]	11
TSPC-based D-FF with AVLS [19]	14
Split-path TSPC-based D-FF	10
Proposed Split-path TSPC-based D-FF with AVLS	13

B. Adaptive voltage level

AVL is a low-power technique used to reduce circuit power consumption. A control signal used to control the AVL circuit. There are two main variants of AVL namely AVLS and AVLG [12]. AVLS decreases the potential of the supply voltage, while AVLG raises the ground potential. From [2] it is inferred that AVLS is preferred over AVLG at higher operating frequencies. AVLS consists of two nMOS transistors and one pMOS transistor as shown in Fig. 3. The pMOS transistor, which serves as the circuit input, is connected to the clock signal. On the other hand, the input of nMOS transistors receives the supply [14].

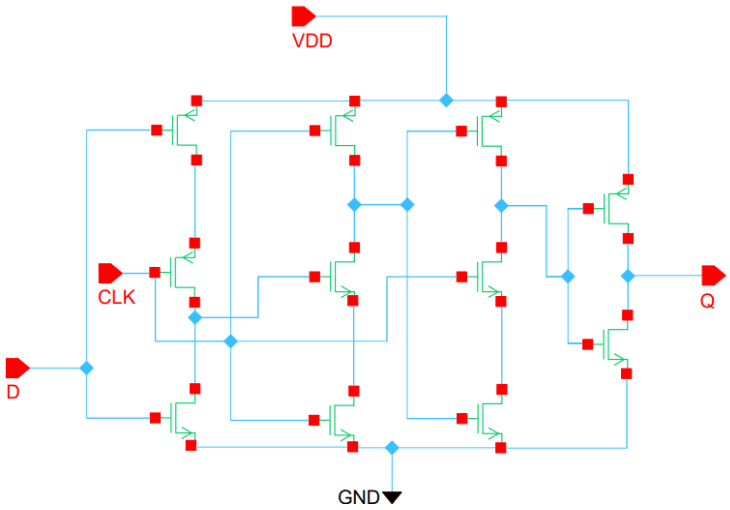

Fig. 1. TSPC-based D-FF circuit

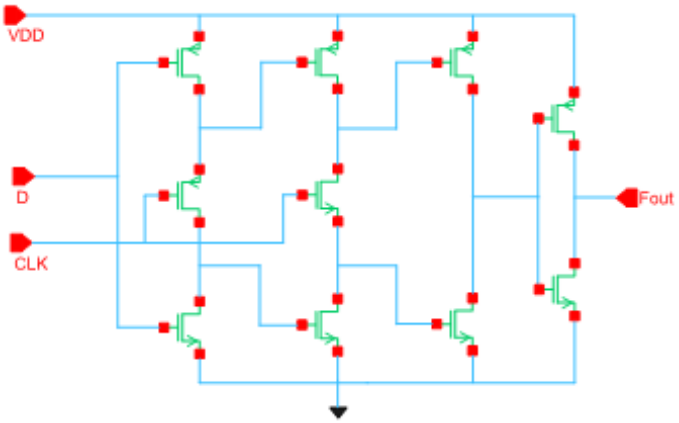

Fig. 2. Split-path TSPC-based D-FF circuit

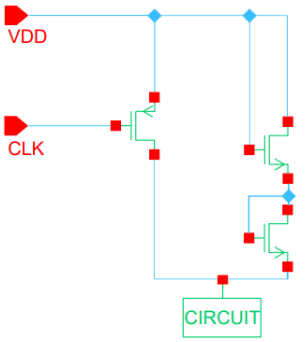

Fig. 3. AVLS circuit

C. Implementation of TSPC based divide-by-32/33 DMPS circuit

The divide-by-32/33 DMPS circuit divides the input frequency by 32 or 33 depending on the control signal. Using create a cell-view option in Cadence Virtuoso, flip-flops, and logic gates (NAND, NOR) are converted into blocks to connect all the components without hassle. Flip-flops and gates are integrated to form divide-by-32 or 33 DMPS. One 2/3 pre-scaler unit, a combination of NAND, NOR gates, and D-FFs are present in the circuit [5]. The 32/33 DMPS circuit has two operating modes: divide-by-32 mode or divide-by-33 mode. When the control signal is logic high, the DMPS operates as a divide-by-32 unit, since the 2/3 pre-scaler operates in divide-by-2 mode. When the control signal is logic low, the 2/3 pre-scaler functions as a divide-by-3 unit, while

the 32/33 DMPS unit functions as a divide-by-33 mode. When the control signal is logic high, the output of NOR2 is logic low, whereas NAND2's output is always forced to be logic '1,' regardless of any data present on the inverted output of D-FF3. The output of NAND2 that is logic high is fed as a control to the 2/3 pre-scaler, the 2/3 pre-scaler operates in divide-by-2 mode, and as a result, the DMPS operates in divide-by-32 mode [16].

The proposed divide-by-32/33 DMPS designs compared with reference 32/33 DMPS circuits in terms of area/transistor count and listed in Table 2. The proposed low-area split-path TSPC-based DMPS with AVLS circuit requires fewer transistors than the circuits in [1] and [19]. The AVLS circuit integrated with the split-path TSPC-based D flip-flop circuit to lower power consumption, as depicted in Fig. 4. Between the source and the existing circuit, AVLS is included. In the proposed-1 design, the two input NOR gates used in the feedback are replaced with equivalent pass transistor logic to minimize the transistor count while maintaining drive strength, as shown in Fig. 5. The regular TSPC-based D-FF is used in this DMPS circuit. Two transistors reduced by using PTL in the proposed-1 DMPS with AVLS circuit; the total number of transistors required is 86, as listed in Table 2.

Table 2. Area comparison of TSPC-based divide-by-32/33 DMPS circuits

Divide-by-32/33 DMPS circuits	Transistor count
Regular TSPC-based D-FF [1]	85
Regular TSPC-based D-FF with AVLS [19]	88
Proposed-1 optimized regular TSPC-based D-FF with AVLS	86
Proposed split-path TSPC-based D-FF	79
Proposed-2 split-path TSPC-based D-FF with AVLS	82
Proposed-3 optimized split-path TSPC-based D-FF with AVLS	80

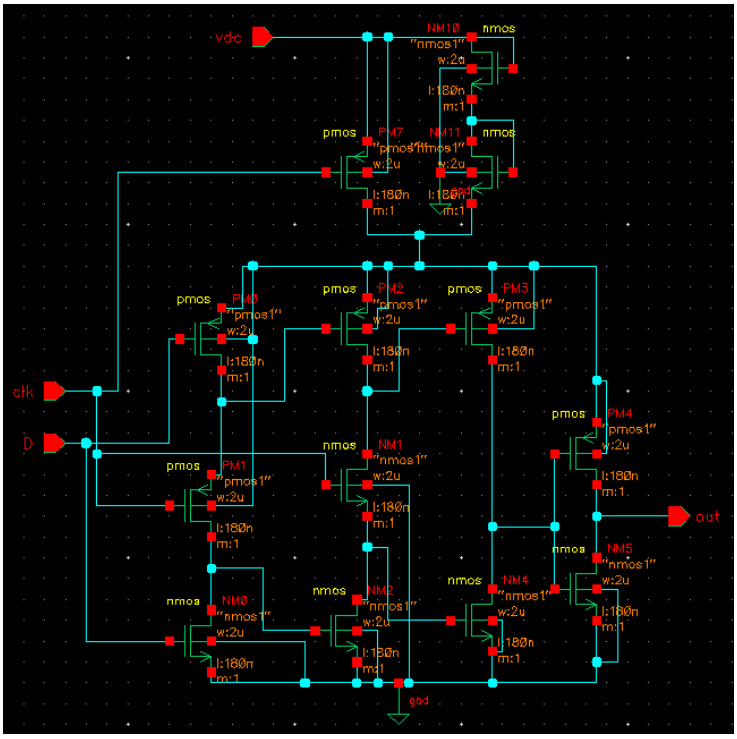

Fig. 4. Proposed split-path TSPC-based D-FF with AVLS circuit

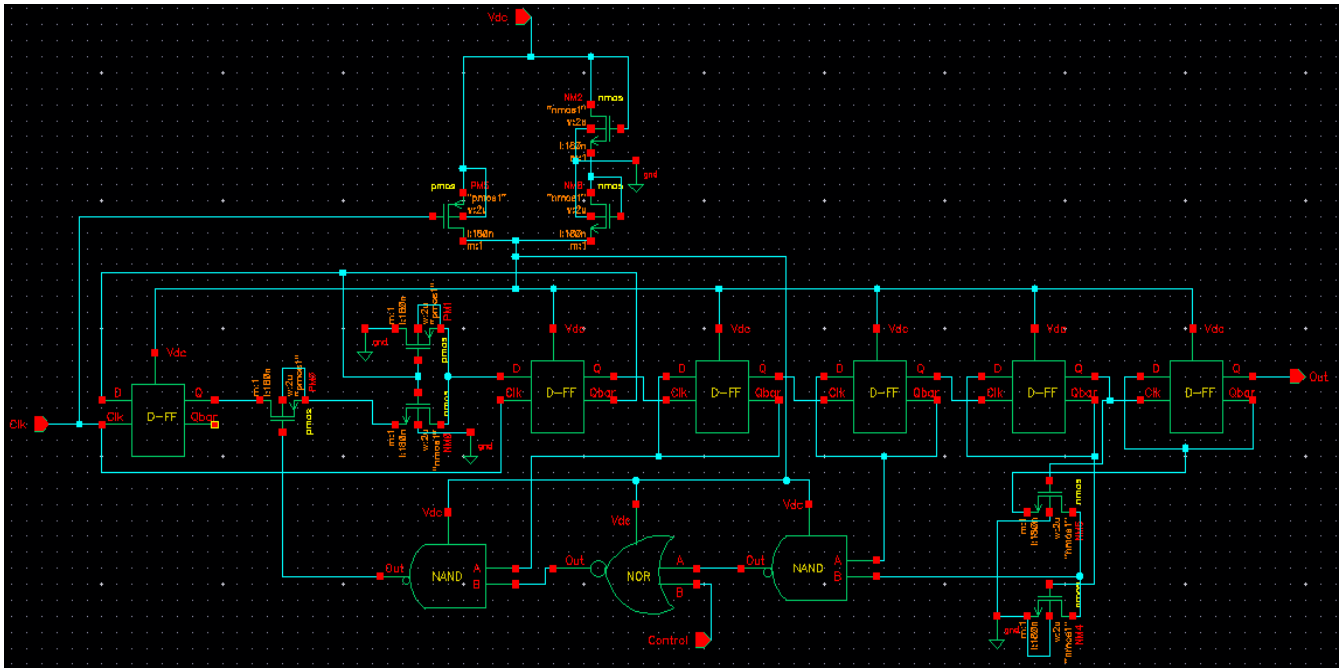

Fig. 5. Proposed-1 optimized divide-by-32/33 DMPS (regular TSPC-based D-FF) with AVLS circuit

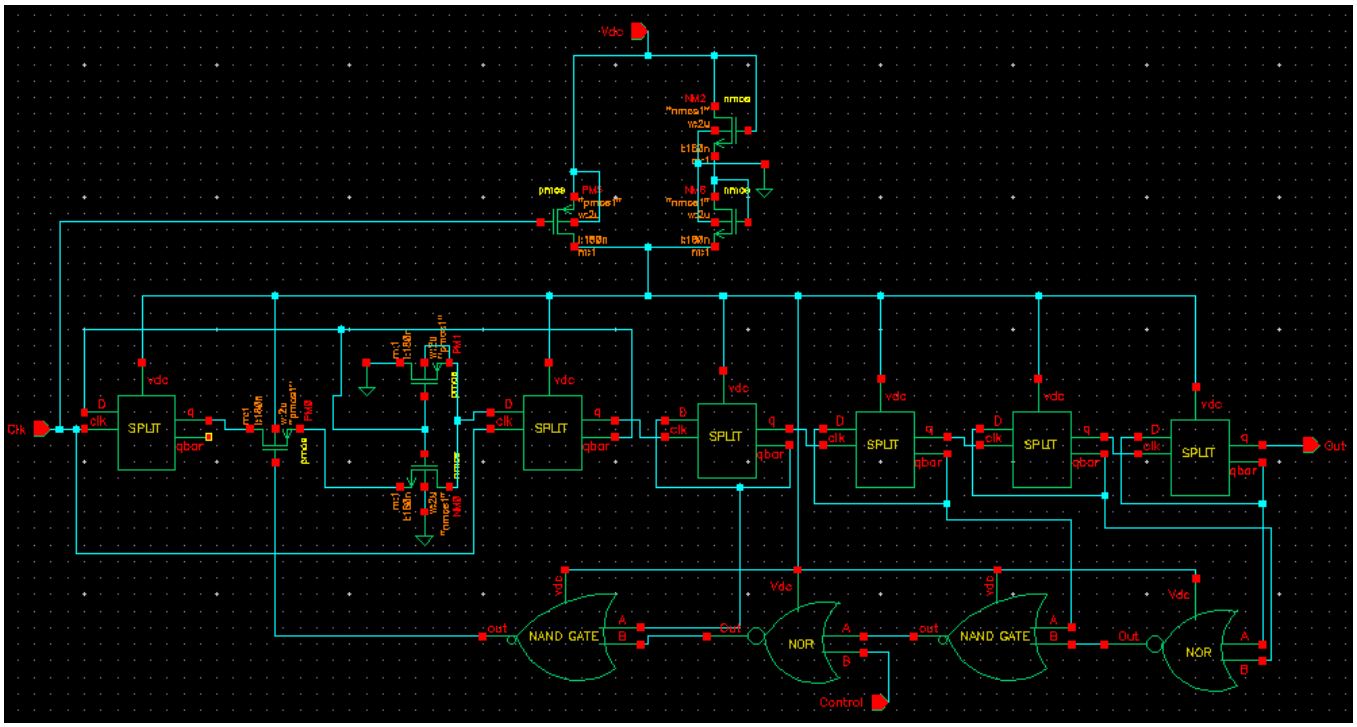

Fig. 6. Proposed-2 split-path TSPC-based divide-by-32/33 DMPS with AVLS circuit

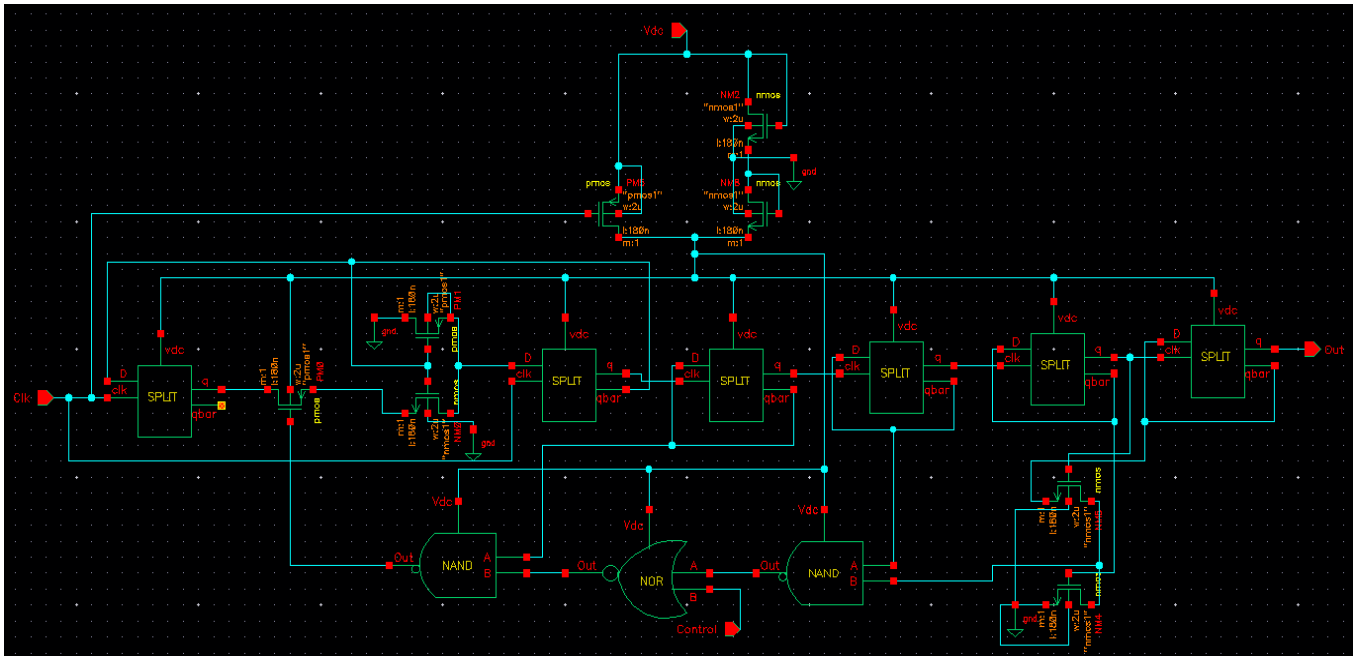

Fig. 7. Proposed-3 optimized split-path TSPC-based divide-by-32/33 DMPS with AVLS circuit

The regular TSPC-based D-FF requires 11 transistors whereas the split-output TSPC-based D-FF requires only 10 transistors. The DMPS circuit consists of six D flip-flops along with the logic gates, a reduction of one transistor in each flip-flop results in a reduction of six transistors in the DMPS circuit. Employing split-path TSPC-based D-FF (in proposed-2 DMPS) leads to a reduction of six transistors. When the AVLS circuit incorporated with the DMPS circuit, the transistor count rises to 82, but there is still a reduction of six transistors compared to the DMPS circuit [19]. The proposed-2 split-path TSPC-based D-FFs and PTL with AVLS circuit is as shown in Fig. 6.

To reduce the area of DMPS further, the NOR gate used in the feedback is replaced with an equivalent pass transistor logic. Hence, in the proposed-3 low-area, 32/33 DMPS based on split-path TSPC-based D-FF integrated with AVLS circuit requires only 80 transistors, as depicted in Fig. 7. Using the proposed-3 DMPS circuit, there is an area (transistor count) reduction of 5.9% compared to DMPS in [1] after employing the low-power (AVLS) technique and a reduction of 9.1% when compared to DMPS in [19]. The proposed DMPS design is area-efficient.

4 Results and discussion

The proposed and existing circuits are realized in CMOS 180 nm/45 nm technology using Cadence Virtuoso. Cadence Spectre used to simulate circuits. The simulations are performed at multiple frequencies and results are verified. In this section, the results are discussed only for the operating frequency at 1 GHz. The power analysis of the various D-FF circuits depicted in Table 3. The values imply that TSPC-based D-FF consumes 51.29µW at 1 GHz, in contrast to transmission gate-based D-FF, which consumes 73.68µW. A reduction of 30.39% in power consumption is observed in TSPC-based D-FF compared to transmission gate-based D-FF. The TSPC-based D-FF with AVLS consumes 13.28% less power compared to the TSPC-based D-FF [2]. The split path-based D-FF utilizes 10 transistors, thereby consuming minimal power, and is 98.56% power efficient when compared to AVLS-based TSPC D-FF as tabulated in Table 3. When implemented in a CMOS 45 nm technology node, a similar trend in power reduction is observed. Both reduction in area (transistor count) and power can be achieved by replacing regular TSPC-based D-FFs with split-output TSPC-based D-FFs.

Power analysis (average of both modes) at various frequencies is performed, and power consumption values at 1 GHz are listed in Table 4 for divide-by-32/33 DMPS circuits. From Table 4, it is evident that the proposed 32/33 DMPS circuits decrease power consumption. In the proposed-3 DMPS with AVLS circuit, a power reduction of 18.85% and 47.78% is observed when compared to DMPS circuits in [19] and [1] respectively. The proposed low-area split-path TSPC-based 32/33 DMPS with AVLS consumes 5.9% less area compared to [1].

The proposed-2 and proposed-3 32/33 DMPS circuits, when implemented in CMOS 45 nm technology node, a power reduction of 41.32% and 46.86% respectively is observed when compared to reference DMPS architecture in [19] as shown in Table 5.

The proposed divide-by-32/33 DMPS circuits consume lesser power, in both modes of operation at 1 GHz operating frequency. The proposed circuits are efficient in terms of both area and power.

Table 3. Power analysis of various D-FFs in CMOS 180 nm technology node at 1 GHz frequency

D Flip-Flop	Average power consumption (μW)
Transmission gate D-FF	73.86
TSPC-based D-FF	51.29
Split path TSPC-based D-FF	0.743

Table 4. Power analysis of divide-by-32/33 DMPS circuits realized in CMOS 180 nm technology node at 1 GHz frequency

Divide-by-32/33 DMPS circuits	Average power consumption (μW)
Regular TSPC-based D-FF [1]	423.75
Proposed split-path TSPC-based D-FF	412.35
Regular TSPC-based D-FF with AVLS [19]	272.7
Proposed-1 optimized regular TSPC-based D-FF with AVLS	269.1
Proposed-2 split-path TSPC-based D-FF with AVLS	224.6
Proposed-3 optimized split-path TSPC-based D-FF with AVLS	221.3

Table 5. Power analysis of divide-by-32/33 DMPS circuits realized in CMOS 45nm technology node at 1 GHz frequency

Divide-by-32/33 DMPS circuits	Average power consumption (μW)
Regular TSPC-based D-FF with AVLS [19]	2.42
Proposed-1 optimized regular TSPC-based D-FF with AVLS	2.389
Proposed-2 split-path TSPC-based D-FF with AVLS	1.42
Proposed-3 optimized split-path TSPC-based D-FF with AVLS	1.286

5 Conclusion

In this paper, the split-output TSPC-based D-FF is used and the AVLS circuit is incorporated to lower the power consumption of DMPS circuits. The proposed low-area split-path TSPC-based divide-by-32/33 DMPS with an AVLS circuit incorporated operates at a higher frequency (GHz). The proposed-1 divide-by-32/33 low-area pre-scaler circuit with AVLS incorporation at 1GHz consumes an average power of 269.1 μW whereas the DMPS circuit in [1] consumes 423.75 μW. There is a reduction in power with a marginal increase in transistor count by 1.18%. The area further minimized by using split-path TSPC-based D-FF. The proposed-3 low-area split-path TSPC-based DMPS with PTL and AVLS improves power efficiency by 47.8% in the CMOS 180 nm technology node. The proposed circuits are also realized in CMOS 45 nm technology and verified the results, a similar trend of power reduction is observed. A power reduction of 41.32% and 46.86% observed for proposed-2 and proposed-3 DMPS circuits respectively. The proposed divide-by-32/33 DMPS architectures have an advantage in terms of both power and area. To reduce power further, other low-power techniques to be explored, such as adiabatic logic as well as transistor sizing.

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