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Design of wide-band high-linearity transimpedance amplifier using standard CMOS technology

Zheng Gu[1], Siqi Wang[2], Chungang Lu[3], Lei Song[3], Zhenghao Lu[4]*, Yonghua Chu[1] and Xiaopeng Yu[2]

In this paper, the design methodology of a high-linearity wide-band transimpedance amplifier (TIA) for cable television (CATV) application is addressed. A simple four-stage topology is proposed to maintain a well-balanced linearity over a wide operating band. The regulated cascode (RGC) input stage is used to match an input impedance of 75 Ω, followed by a gain stage with enhanced bandwidth. The high-linearity output stage is able to drive the 75 Ω load directly with high output swing under a high supply voltage. The prototype is implemented with a standard 0.11μm CMOS process while occupying the silicon area of 0.034 mm^2. The measurement results for the prototype show a peak gain of 76.6 dBΩ over a 3-dB bandwidth of 1.1 GHz with a considerably small gain ripple and an OIP_3 of 20.4 dBm. The whole test chip consumes 447 mW DC power and the measured average input-referred noise current spectral density is 7.9 pA Hz$^{-1/2}$ up to 1 GHz.

Keywords: CMOS, CATV, transimpedance amplifier, high linearity, sensor interface, regulated cascode

1 Introduction

For decades, transimpedance amplifiers (TIAs) have been widely exploited as the key front-end circuits for optical sensors, and communications, which with no exception, entails many design trade-offs among the noise, bandwidth, gain, dynamic range, supply-voltage, and power dissipation. Traditionally, obtaining sufficient bandwidth with small gain ripples and acceptable input-referred noise is of the first priority due to the limited f_T of CMOS technology. With the rapid progress of nowadays nano-scale CMOS technology, however, the challenges in operating frequency have been solved effectively. Many designs working with tens of Gbps have been reported extensively, which also include many design techniques such as inductive peaking, the regulated cascode (RGC), noise canceling, etc [1-14]. However, as a complex analog building block, several challenges still remain. In the application of fiber-to-the-home (FTTH) based cable television (CATV), the input photoelectric current signal contains up to several tens of channels. With so many channels modulating with each other, the intermodulation component will cause serious interference to the desired channel. As the first stage of the analog front-end, without the existence of a band selection filter, poor linearity of TIA will greatly deteriorate the sensitivity of the system even if the input-referred noise has been reduced to a considerably low level [15]. Moreover, the TIA usually works as a small signal amplifier, which only provides very limited drive capability especially advanced CMOS technology with low supply voltage. It will be preferred if the circuit can also provide a large output swing for industrial applications.

In this paper, the design techniques focused on low cost, high linearity, and high drive capability have been reviewed. A transimpedance amplifier implemented with 0.11 μm CMOS process is proposed to achieve a well-balanced among the noise, bandwidth, linearity, silicon area, etc. The manuscript is organized as follows. Section 2 introduces the detailed implementation of the proposed design, which includes an RGC input stage, a buffer stage, a wide-band gain stage, and an output stage. Section 3 addresses the details of the layout and chip implementation, followed by measurement results. The conclusion is given in Section 4.

2 Circuit implementation

Figure 1 shows the architecture of the proposed design, which includes an input stage of RGC with a source follower, a gain stage, and an output driver. The circuit is optimized as a wide band, low noise, high linearity, output swing, and small silicon area. The major bottleneck of wide-band operation lies in the large input

[1] The Second Affiliated Hospital of Zhejiang University, School of Medicine, Hangzhou 310027, China
[2] Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China
[3] Marketing Service Center, State Grid Zhejiang Electric Power Limited Company, Hangzhou, China
[4] Soochow University, Department of Microelectronics, Suzhou 215031, China
* luzhh@suda.edu.cn

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capacitance. To achieve low noise, the first stage should be low noise and able to provide a considerably large gain. Moreover, the circuit is implemented with the differential form to achieve better noise performance. The output stage is optimized with high linearity since it is the dominant factor. Moreover, to make the drive capability as high as possible, a high output swing is greatly desired. In the work, a standard 1.2/3.3 V 0.11 μm CMOS technology is used, it is possible to use a supply voltage of 5 V so that it can be used to drive many applications such as sensor interfaces. The transistors and resistors of the output stages are carefully sized so that the voltage drop between all the terminals of the transistors is below 3.3 V. The functionalities of these blocks are described in detail.

The regulated cascode (RGC) input stage, as shown in Fig. 2(a), is a more suitable candidate for wide-band applications. Thanks to the advantage of incorporating strong local negative feedback, we can realize impedance matching with very low power cost. As a result, the impact of large input capacitance including the photodetector capacitance can be significantly reduced. Therefore, unlike common gate or common source TIAs, the dominant pole of an RGC TIA is usually located within the amplifier rather than at the input node [10]. The input impedance of the RGC stage could be derived from the small-signal circuit model shown in Fig. 2(b) as

$$Z_{in}(s) \approx \approx \frac{\left(\frac{1}{R_2}+sC_j\right)}{\left(g_{m2}+\frac{1}{R_2}\right)\left(g_{m1}+sC_j\right)+\left(\frac{1}{R_2}+sC_j\right)\left(\frac{1}{R_s}+sC_i\right)} \quad (1)$$

where $C_i \approx C_{sb1}+C_{gs2}$ and $C_j \approx C_{gs1}+C_{gd2}$. The low-frequency small-signal input resistance is given by

$$R_{in}=Z_{in}(0)\approx\frac{1}{g_{m1}(1+g_{m2}R_2)} \quad (2)$$

As you can see from Eqn. (2), compared to voltage-mode TIA, we can match the DC impedance of the RGC to 75 Ω at the expense of a relatively low current consumption compared to voltage mode TIA.

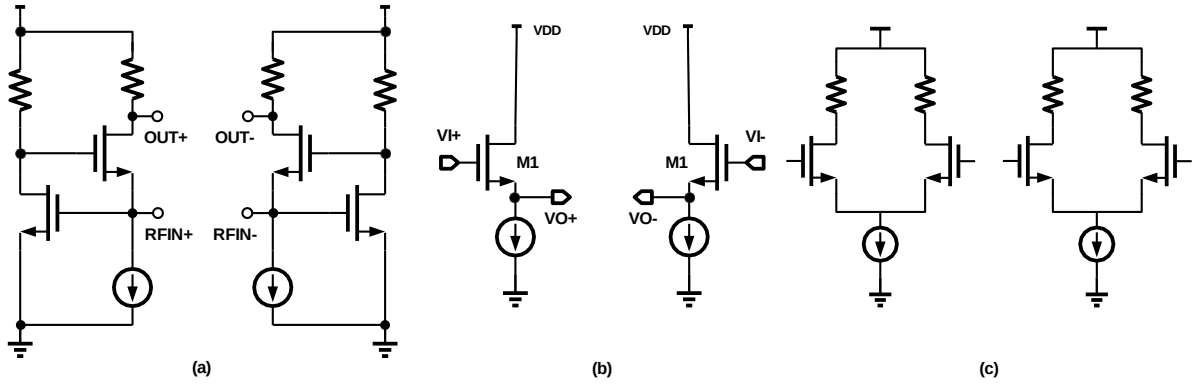


Fig. 1. Architecture of the proposed TIA

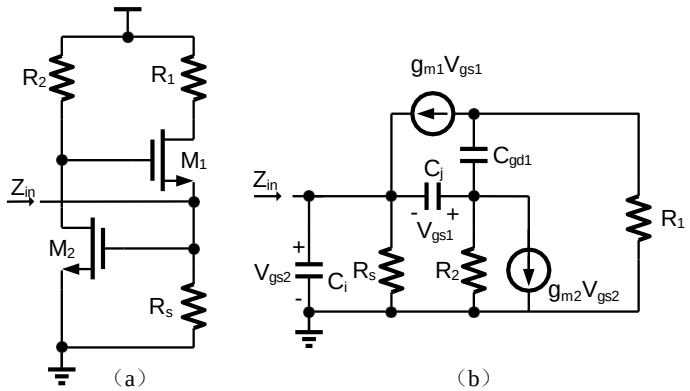


Fig. 2. Regulated cascode stage: (a) its circuit schematic. (b) its small-signal model

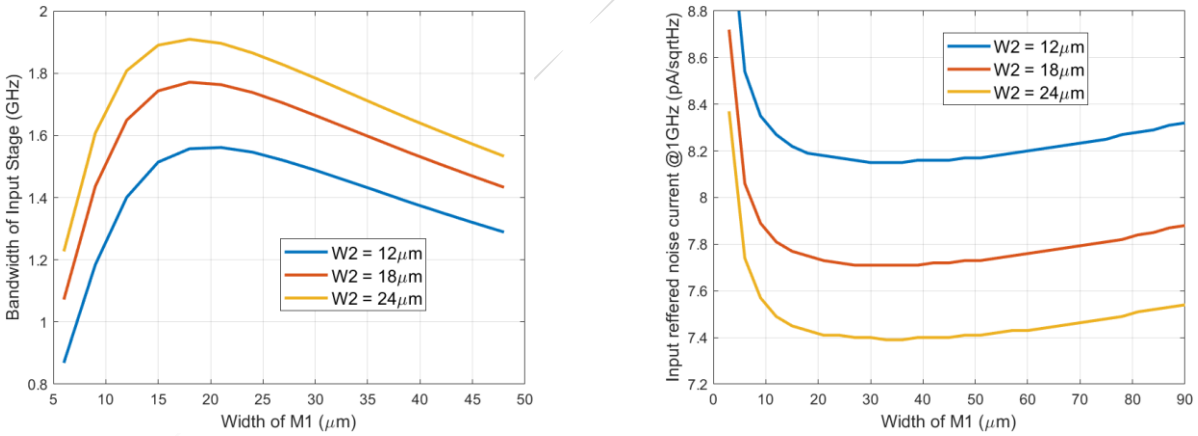
In addition, the local feedback formed by M_2 and R_2 introduces a zero, which will cause peaking in frequency response. The frequency of zero is given by

$$f_z = \frac{1}{2\pi R_2 (C_{gs1} + C_{gd2})}. \quad (3)$$

To limit the peaking effect, it is clear that the width of M_1, M_2, or resistance R_2. should be reduced. However, reducing W_2 or R_2 will decrease the loop gain of local negative feedback, which increases the input impedance. Also, smaller W_1 leads to larger impedance. Therefore, both M_1 and M_2 should be carefully sized. The simulated relationship of RGC bandwidth versus the size of M_1 and M_2 is shown in Fig. 3(a). It is shown that, as the size of M_1 increases, the bandwidth of the input stage first increases and then decreases due to the peaking effect. It is also worth noting that an oversized M_1 will directly increase the input capacitance of the TIA, thus limiting the bandwidth.

Another advantage of using RGC as an input stage is its excellent noise performance. Thanks to the existence of negative feedback, the noise contributed by M_1 is divided by $(1+g_{m2}R_2)$ compared to the conventional common gate (CG) input stage. That is, in order to get the same noise performance, the CG structure needs to increase the size of M_1 or increase its bias current. This will undoubtedly make the input parasitic capacitance increase, or consume more power.

Based on the analysis in [13], in order to minimize the minimum input equivalent noise current of the RGC, the width of M_1 and M_2 need to satisfy the following conditions, (i) $C_{gs2} = C_{in} + C_{sb1}$, (ii) $C_{gs1} = C_{gd2}$, where C_{in} is the input parasitic capacitance including the photodiode and bonding pad. Figure 3(b) shows the simulation result of input-referred noise at 1 GHz while sizing M_1 and M_2. However, due to the technology limitations and the relationship between gain-bandwidth and noise. It is usually not possible to achieve the optimum noise performance while maintaining the required gain-bandwidth. We still need to make a trade-off between the noise and the transimpedance gain bandwidth of the RGC stage to get a balanced performance. In this work, the transistor widths of M_1 and M_2 are chosen to be 24 µm and 18 µm, and the resistance of R_1 and R_2 are both 2 kΩ.



(a) (b)

Fig. 3. Simulated performance of RGC versus size of $M1$ and $M2$: (a) Bandwidth, (b) input-referred noise

The input stage of RGC induces a large transimpedance, which may result in a low-frequency pole. It is, therefore, necessary to add an isolator between the input stage and gain stage as shown in Fig. 4(a). The small signal of the source follower is shown in Fig. 4(b). The small signal gain of the circuit is given as

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m} \quad (4)$$

The zero is in the left-half plane, and the dominant pole with $R_s = 0$ is:

$$\omega_{p1} \approx \frac{g_m}{g_m R_S C_{GD} + C_L + C_{GS}} = \\ = \frac{1}{R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}} \quad (5)$$

The circuit has no gain but it offers a well-defined buffer between the input impedance and gain stage so that the bandwidth of the whole TIA will not be limited by the high impedance of the input stage. The gate of the source follower is RC coupling to the output node of RGC. The RC high-pass frequency corner is designed to be 3 MHz, which is ten times lower than the minimum frequency of our application.

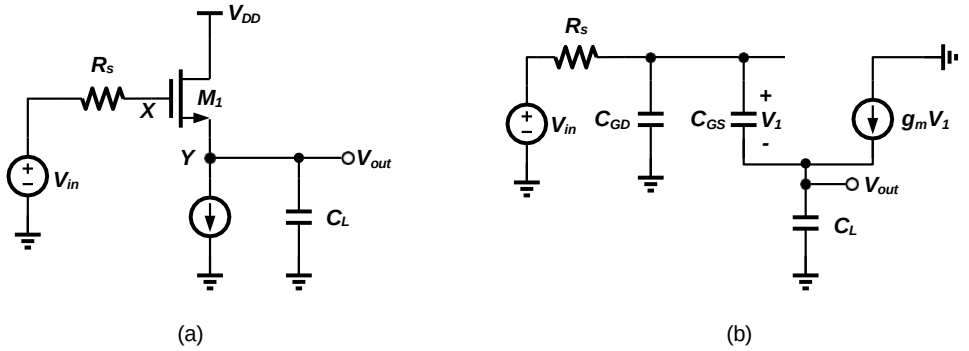


Fig. 4. Isolator between input and gain stage: (a) its circuit schematic, (b) its small-signal model

The third stage of the TIA is optimized with a high gain as shown in Fig. 5(a) (for simplicity, only the half-circuit is shown), while the small signal model of the common source amplifier is shown in Fig. 5(b) [14]. The voltage gain of the common source stage is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1}, \quad (6)$$

where $\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB}$. The voltage gain of the amplifier depends upon the transconductance g_m, the linear resistor R_D, and the load. In order to increase the gain, we have to increase the g_m as well as another important factor, the load impedance connected to the output. For a given technology, the gain-bandwidth of the gain stage is limited by the transconductance of the transistor, which can be improved at the expense of power consumption. The circuit is properly sized to achieve a sufficient gain up to 1 GHz range.

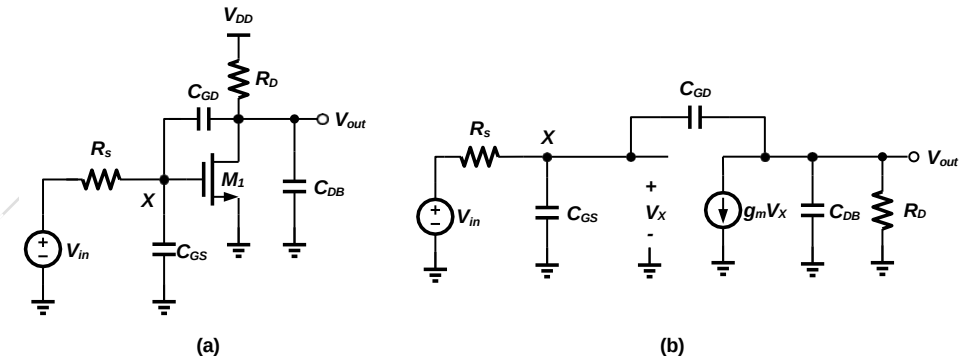


Fig. 5. The gain stage of the proposed design: (a) its circuit schematic, (b) its small-signal model

The final stage is the output buffer, which is designed to drive 75 Ω off-chip load. As the last stage of the whole circuit, the linearity of the output buffer is the major bottleneck [15]. Suppose the system is subject to a two-tone blocker with an amplitude of P_B in dBm. This results in an undesirable inter-modulation component IM_3 whose level in dBm is

$$IM_3(\text{dBm}) = 3P_B - 2IIP_3, \quad (7)$$

where IIP_3 is the input third-order intercept point.

In this scenario, the minimal detector signal should be higher than the interference and noise with a certain SNR., which makes the sensitivity of the receiver to be

$$Sensitivity = 3P_B - 2IIP_3 + SNR \tag{8}$$

The equation indicates that the noise figure is not the only parameter that decides the sensitivity of the analog front end in the presence of a strong interference signal. It is highly desired to make the linearity as high as possible if the input signal is subject to strong near-band interferences. In this work, to achieve this target, the output stage is designed to be differential as shown in Fig. 6 to improve IIP_2. The differential circuits exhibit "odd-symmetric" characteristics since the even-order terms in the polynomial are canceled out.

Consider two amplifiers providing equal small-signal voltage gain of [14]

$$|A_v| \approx g_m R_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) R_D \tag{9}$$

If an input $V_m \cos(\omega t)$ is applied to each circuit, for the common stage, then

$$\begin{aligned} I_D &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} + V_m \cos\omega t\right)^2 \\ &= I_{D0} + \mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)V_m \cos\omega t + \frac{1}{4}\mu_n C_{ox}\frac{W}{L}V_m^2[1+\cos(2\omega t)] \end{aligned} \tag{10}$$

For the differential pair, it can be shown that

$$I_{D1} - I_{D2} = g_m\left[V_m - \frac{3V_m^3}{32(V_{GS} - V_{TH})^2}\right]\cos(\omega\, t) - g_m\frac{V_m^3\cos(3\omega t)}{32(V_{GS} - V_{TH})^2} \tag{11}$$

$$\frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2} \tag{12}$$

The equations indicate that the effective way to improve the linearity is to increase the supply voltage and optimize biasing condition at the expense of power consumption. In this work, since the large output swing is desired, a 5 V supply voltage is used. Of course, the DC biasing condition should be properly defined so that the voltage drops among all the terminals of transistors are within 3.3 V.

To achieve output impedance matching, the drain resistor is designed to be 75 Ω, which is specified for CATV applications. According to Eqn. (12), the amplitude of the third harmonic is inversely correlated with the overdrive voltage of the input differential pair. This means that the relative current swing of the output stage can be reduced by increasing the overdrive voltage of the differential pair, thereby increasing the output intercept point (OIP_3) of the output stage. It is shown in Fig. 7(a), as V_{GS} increases, OIP_3 first gradually increases. However, because the input DC voltage of the input differential pair is determined by the front stage, which means that the maximum V_{GS} is limited. In other words, the transistor of the tail current will enter the linear region, while the size of the differential pair is too small. The contour in Fig. 7(b) illustrates the linearity of the output stage as a function of the biasing current and transistor size. Therefore, we traded off the area and power consumption of the chip and determined the width of the input pair to be 90 μm with biasing current 60 μA.

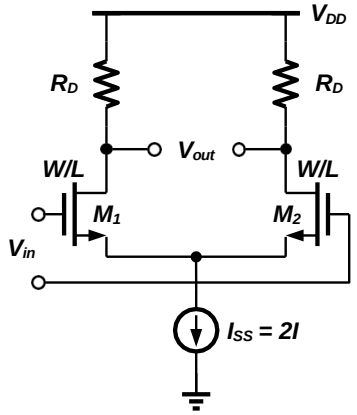
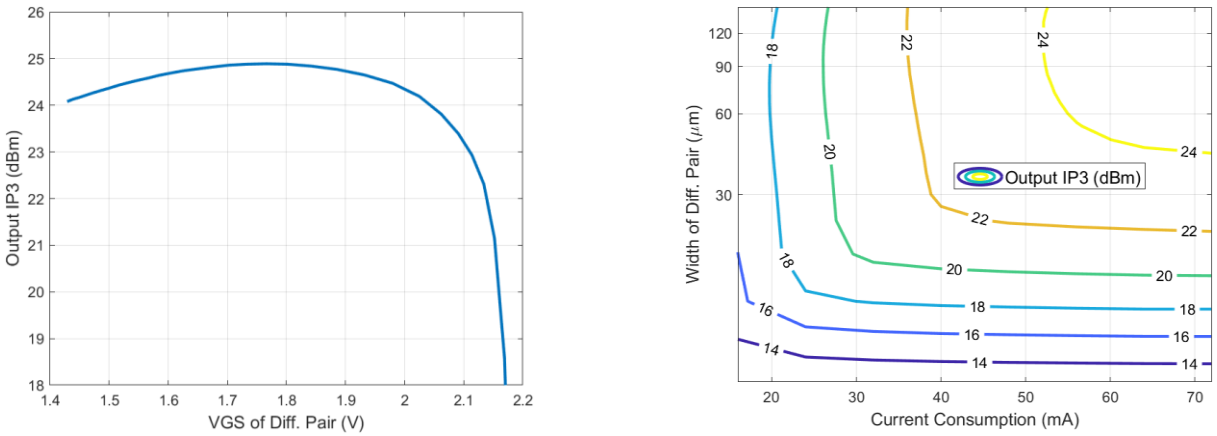
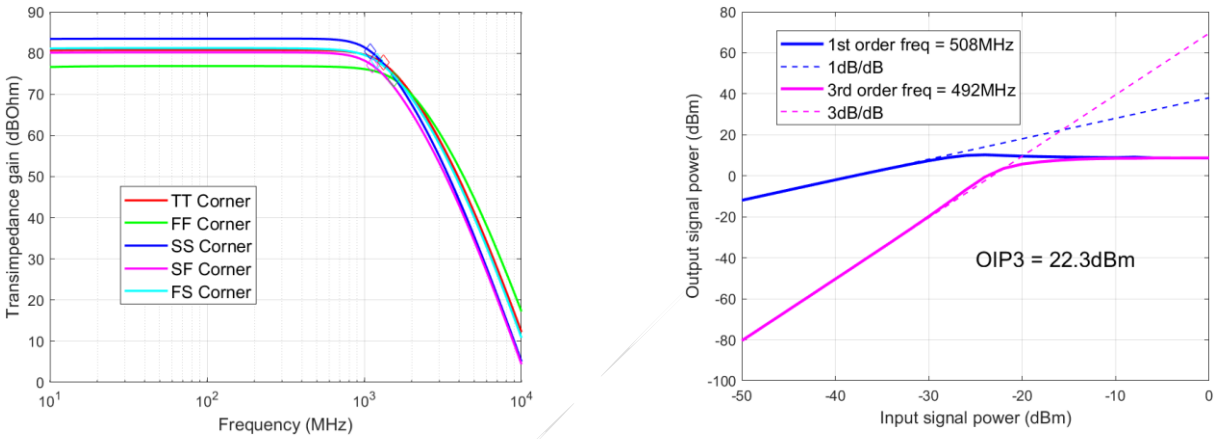


Fig. 6. The topology of output stage



(a) (b)

Fig. 7. Simulated output intercept point (OIP_3) *versus*:
(a) V_{GS} of differential pair, (b) the size and power of differential pair



(a) (b)

Fig. 8. Post-layout simulated performance of proposed TIA:
(a) Transimpedance frequency response, (b) output IM3 *versus* input signal

3 Simulation and measurement results

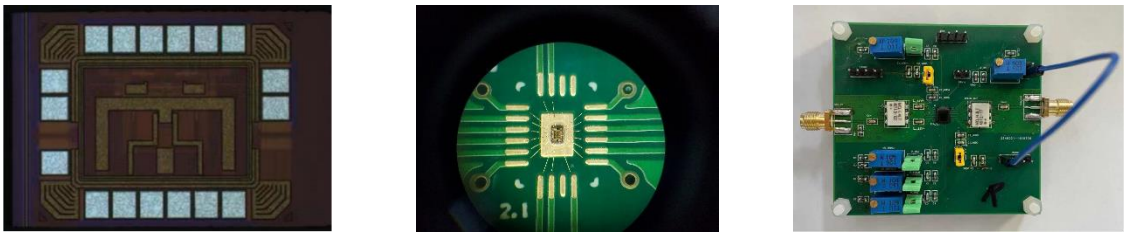
The simulations of the proposed TIA design are performed using the Cadence IC SpectreRF and HHGrace 0.11 μm CMOS design PDK. Small adjustments and fine optimizations on the device sizes with the help of the circuit simulator are necessary to meet the design objectives. The final overall gain distribution is as follows: the first stage (RGC) provides a transimpedance gain of 72 dBΩ, and the second, third, and output stages provide voltage gains of –2 dB, 8 dB, and 3 dB, respectively. Therefore, comes to a total transimpedance gain of 81 dBΩ.

The transimpedance gain frequency responses among different corners are shown in Fig. 8(a) by post-layout simulation. The gain variation of the proposed TIA ranges from 77 dBΩ to 83 dBΩ and the bandwidths are all above 1 GHz. The variation in transimpedance gain mainly arises from the different resistance values of the load resistor in the RGC stage. In further work, an AGC loop can be added after the TIA stage to eliminate the gain variation. Figure 8(b) shows the simulated output intermodulation distortion. The third-order intermodulation (IM_3) curve shows that the OIP_3 is 22.3 dBm, which is high enough for our application.

A prototype of the design is fabricated in HHGrace 0.11 μm CMOS. Figure 9 shows the die photo of the test chip, the test chip with bonding wires, and the PCB of the prototype. The core area of the proposed TIA is only 180×190 μm^2. The chips are packaged and measured in the form of COB. The measured current consumptions are 33 mA from 4 V supply and 63 mA from 5 V supply. The total dc power of the proposed TIA is 447 mW.

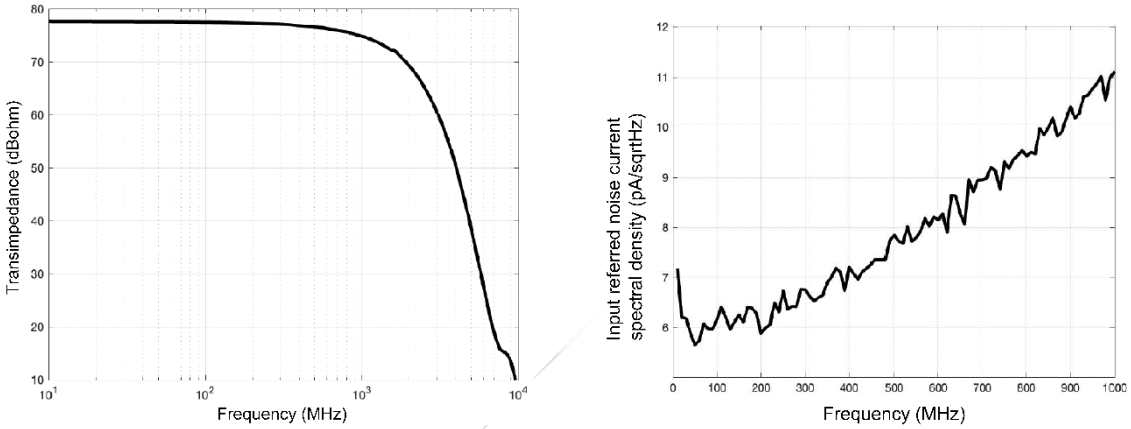
The frequency response is measured with HP8510C network analyzer. The measured transimpedance frequency response of the proposed design is shown in Fig. 10(a). The transimpedance gain frequency response

exhibits a –3 dB bandwidth of about 1.1 GHz and 77.6 dBΩ transimpedance gain with a very small gain ripple. Compared to the simulated result in Fig. 8(a), the low-frequency gain matches well while at higher frequencies the measured gain drops faster than simulated, which is possibly due to the non-ideality of the onboard balun, the EM radiation loss, the silicon substrate loss, and process variations.



(a) (b) (c)

Fig. 9. Photograph of the proposed TIA: (a) Die photo, (b) chip bonding, (c) Testbench PCB



(a) (b)

Fig. 10. Measured performance of proposed TIA:
(a) Transimpedance frequency response, (b) input-referred noise

Fig. 11. Measured intermodulation components of two-tone testing

The measured noise response is shown in Fig. 10(b). The noise measurement is carried out using 8970B Noise Figure Meter, 8971C Noise Figure Test Set, and NP5B Noise Parameter Test System. The average measured input referred noise current spectral density is about 7.9 pA $Hz^{-1/2}$ and the total input referred noise current is 245 nA integrated up to 1 GHz. The measured input referred noise current spectral density is higher than the simulated one, possibly due to additional parasitic elements and substrate noise/losses that are not

considered in the simulation and process variations. Figure 11 is the output spectrum of two-tone testing. The measured main tone power output is about –5 dBm and IM3 component power is –55.8 dBm. This translates to an actual output intercept point of 20.4 dBm, which is smaller than the result of post-simulation. One possible reason for this may be the inaccuracy of the large signal nonlinearity model in circuit simulation.

4 Conclusion

In conclusion, a wide-band transimpedance amplifier (TIA) with high linearity and high output swing is proposed for CATV application. The design includes an RGC input stage with a source follower buffer, followed by a gain stage. The gain stage and output buffer stages are optimized with high linearity to improve the in-band interference rejection. A prototype of the proposed design implemented with 0.11 μm CMOS process. Measurement results show a 3 dB bandwidth of about 1.1 GHz with a very small gain ripple and an OIP_3 of 20.4 dBm. The transimpedance gain is 77.6 dBΩ. The chip consumes 447 mW DC power and the measured average input-referred noise current spectral density is 7.9 pA $Hz^{-1/2}$ up to 1 GHz. Comparisons with published results demonstrated an improvement in terms of linearity as shown in Table 1.

Table 1. Performance comparison with previous works

Parameters	This work	TMTT [3]	Rafael RT990 [16]	TCAS-I [4]	TCAS-II [5]	TCAS-I [8]
Tech (nm)	110	65	/	130	180	65
3-dB Bandwidth (GHz)	1.1	6.5	1	0.01	1.75	0.08
Transimpedeance gain (dBΩ)	77.6	56.3	41	100	48.6	15
Noise (pA $Hz^{-1/2}$)	7.9	15.1	/	2.7	2.4	/
Current consumption (mA)	96	7	150	0.3	27	7.9
Supply voltage (V)	4/5	1.3	5	1.2	1.8	1.8
OIP_3 (dBm)	20.4	/	22.5	/	/	26.8
Core Area (mm^2)	0.034	0.037	0.16	0.2	1.45	0.037/0.258

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