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A SWITCHING TECHNIQUE FOR VOICE COMMUNICATION OVER EXISTING COPPER INFRASTRUCTURE

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In this paper a technique for the switching of voice communication over existing cabling is described. For example, an existing physical layer like the power grid infrastructure of a building can be used for voice transmission. The hardware implementation and the associated protocol implemented on a microprocessor are described. For such a preinstalled physical medium, the use of a voice communication switch or exchange (PBX) is obviously not applicable. The paper deals with the development of a "distributed" exchange, capable of switching voice in as many as 30 subscribers. Each user is allocated a time slot, which acts as a private mailbox. The switching is based on the principle of Time Slot Interchanging (TSI). The necessary modifications to the basic idea of TSI are described and the whole design, including the required protocol, is given.

K e y w o r d s: time slot interchange, power line modems, voice exchange, HDLC protocol

1 INTRODUCTION

Nowadays it is very common to adopt packet switching techniques in order to use more efficiently the available capacity of any physical medium. Usually, it is not considered as state of the art to allocate time slots, like in Pulse Code Modulation (PCM) systems, for each user. On the other hand there exist commercial applications like the so-called Digital Pair Gain Systems where the technique of allocated time slots is adopted. In our case the hardware interface developed, makes capable the connection of analog telephone sets to an existing two-wire bus, like the power network. Adopting the European PCM Standard (E1), we can provide voice connectivity and switching to as many as 30 users. As this kind of network is already available at no cost, it is not of high priority to use the network bandwidth as efficiently as possible. Also, as our application is to transfer voice, a packet switching technique could be vulnerable to delays of packets or loss of packets, *ie* reduced quality of service. For the above reasons we choose to implement the access to the copper infrastructure by means of time slots allocated to a limited number of users.

The switching is based on the principle of Time Slot Interchanging (TSI). This technique is described in Figure 1. This figure, mainly adopted from [1], shows the sampling and multiplexing procedure and the A/D conversion at the transmitter side for N subscribers. If a direct connection to the receiver end were established, considering also fixed synchronization to both switches/multiplexers the single channel shown by the dashed line would carry N signals at the same time without any provision of switching. In order to provide switching an intermediate storage and retrieval of samples in digital form takes place. According to this well-known technique, the samples are stored sequentially in the Slot Content Memory, as this memory is addressed by a counter (Time Slot Counter). The switching is provided by the way that this memory is addressed when is being read. The reading is not sequential but instead it is done by means of another memory, the Control Memory, where the information regarding the present connectivity status is stored. The contents of this memory are the addresses of the first memory and is usually a part of the switching center. The idea described in this paper is that this memory physically does not exist, but instead its content is circulated among all subscribers in a specific time slot sequence. For this purpose the High Level Data Link Control (HDLC) protocol is adopted. According to this, Figure 2, the PCM stream (layer-1), divided in 32 time slots, 8-bits each, reserves one time slot (S in Fig.2) for signaling. These S time slots when collected and combined construct the so-called S-channel. This channel carries the HDLC protocol as shown in the upper part of Fig.2. In a standard implementation there is a flag at the beginning and a second one at the end, an Address field, a Control field, a CRC field as well as an Information field. The latter is the one that replaces the Control Memory of traditional Time Slot Interchange technique.

2 MEDIUM ACCESS PROTOCOL

In this paragraph the protocol used for the access to the common medium is described. The medium is considered as a two-wire bus. Each station is assigned a unique time slot, in time division format, that can be considered as private mailbox where the information concerning the specific station is delivered by another party (station). The time slot is associated to the station even if there is no information to be transferred. Actually the bus is considered as a PCM bus, and all the functional characteristics of the European E1-PCM system have been adopted. This is very convenient, as many hardware parts are directly available. On the other hand the S-channel is dynamically handled. The protocol running on this channel

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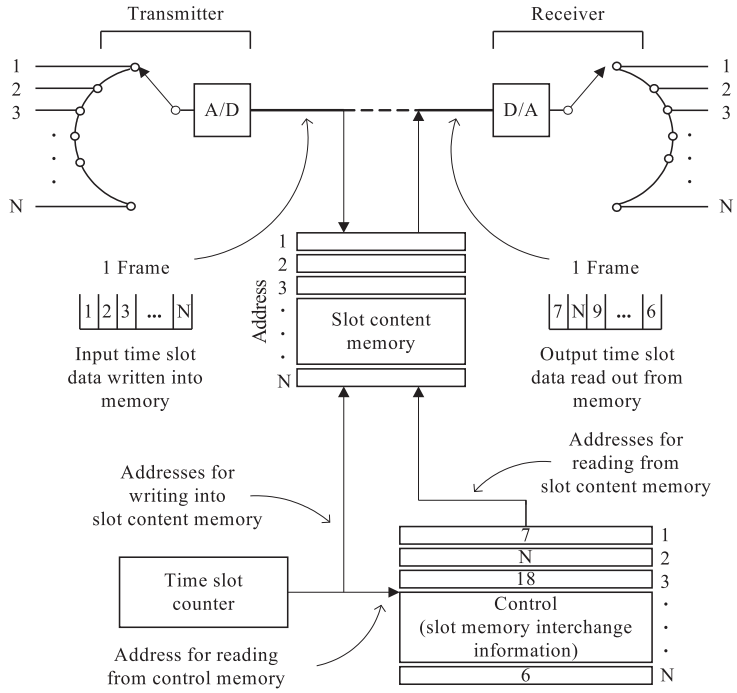

Fig. 1. Time Slot Interchange (TSI) switching technique

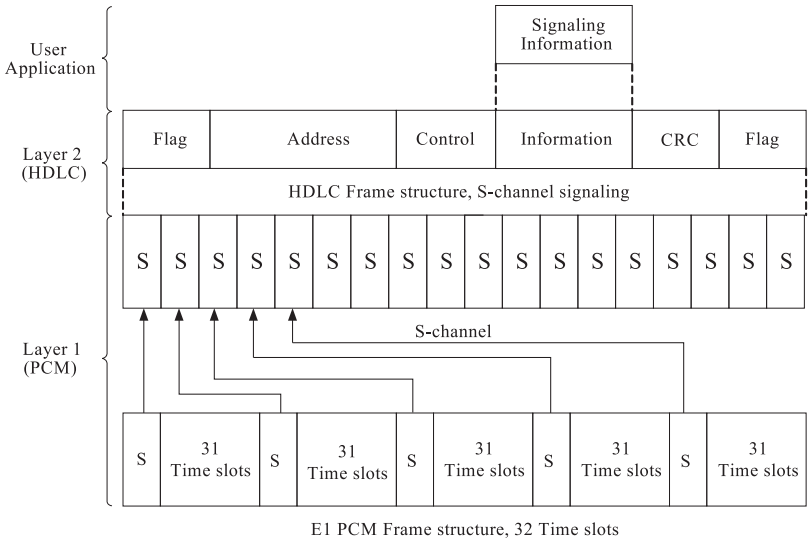

Fig. 2. HDLC protocol runs on S-channel, which comprises S-time slots of sequential PCM frames [2]

manages the access to the common medium and is based on a token passing technique. The token is a unique control frame, which is circulated sequentially to all stations involved in this configuration. The station that possesses the token is able to transmit control and signaling information on the Control channel (S-channel). This channel is constructed from the 16-th time slots of the sequential PCM frames and carries two types of frames: Signaling Frames and Control Frames.

The Signaling Frames are used for the transfer of data regarding the access of stations to the medium, *ie* who is communicating with whom in analogy to the Control Memory of the TSI system. The Control Frames manage the access to the medium. Both kinds of frames use the structure of HDLC protocol, which is supported by the processor involved. Figure 3 shows the flow diagram of the several states that a station can pass through.

3 FRAME STRUCTURE

The HDLC frame is shown in Fig. 4. The receiver address field, 1-byte long, contains the address of the station to which the control message is to be delivered. This must not be confused with the time slot associated with each station where the voice samples are delivered.

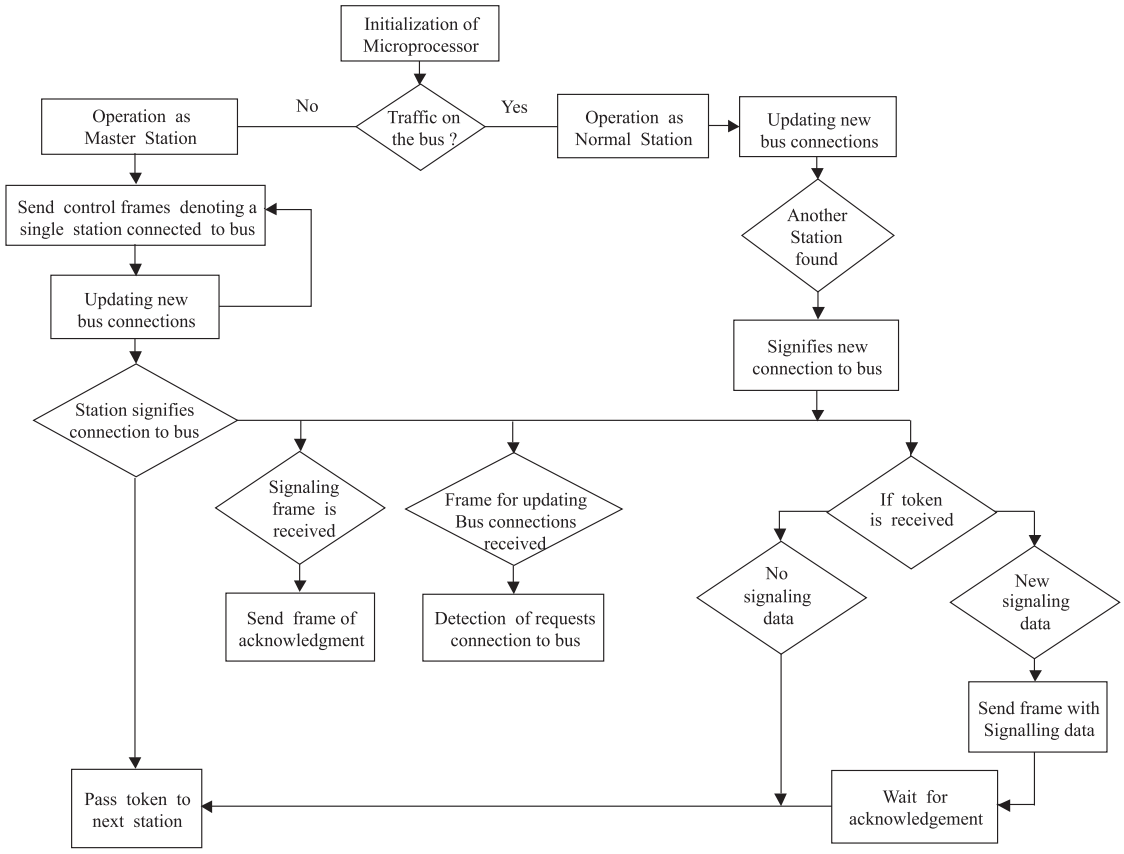

Fig. 3. Flow diagram of the various states of the stations

According to the protocol, each station reads this field to decide if it is the intended recipient of the frame. The sender address field is also 1-byte long and as the name implies, contains the address of the sender, in order for the receiver station to know which station sends the information.

When a station intents to transmit a signaling frame to another station, it waits until it receives a control frame which transfers the token to it. As soon as the token is received, the station first transmits its data and switches in a receive mode waiting for a reply from its partner station. A stop and wait technique is utilized in order to regulate the flow of information among stations.

Access to the Medium

When a new station is connected for the first time to the medium (two-wire bus) it switches to receive (Normal) mode. The station listens the bus traffic in order to find out if there is any other station connected. If the station realizes that is the first one that is connected (no traffic on the bus) it identifies itself as Master Station and periodically transmits a control frame in order to warn the next stations that this is the only one active (solicit successor). The second station listens for a specified period of time if any transmission takes place and as soon as it realizes that there is a Master Station, it identifies itself as Normal Station. These two stations exchange the token between them, giving rise to a bus traffic. Any other new station connected, listens to the bus traffic and remains in Normal mode. Each new station reads the address field in the transmitted control frame and recognizes which is the transmitting station.

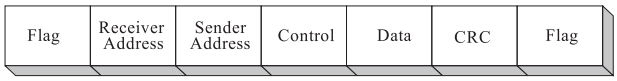

Fig. 4. Structure of an HDLC frame

The connected stations on the bus form a logical ring and allow periodically any new stations to be connected. Finally, as far as the S-channel is concerned, all the stations are in a wait mode detecting an attempt of a new connection. The addresses, *ie* the logical positions of the stations on the logical ring are stored in the microprocessor's memory in the form of a matrix (Matrix of Connected Stations, MCS). In this way each station knows which other stations are connected and it is possible to exchange data. In Table 1 the values of the control and data fields of the frames that are exchanged are shown. In Table 2 the signaling frames are also given.

Table 1. Control Frames of the HDLC Protocol

VALUE	HDLC FIELD	REMARKS
C	Control	Defines a control frame
SS2	Data–CF	Signifies bus connections updating
T	Data–CF	Signifies the token passing
SS1	Data–CF	Signifies a single station on the bus
BES	Data–CF	Signifies a station connecting to the bus
SES	Data–CF	Signifies a station exiting to the bus
R	Data–CF	Signifies data reception without errors
E	Data–CF	Signifies data reception with errors

CF–Control Frame

Table 2. Signaling Frames of the HDLC protocol

VALUE	HDLC FIELD	REMARKS
S	Control	Defines a signaling frame
CREQ	Data–SF	Connection Request
CRES	Data–SF	Connection Response
BUSY	Data–SF	Busy State
CCON	Data-SF	Connection Confirmation
DREQ	Data-SF	Disconnection Request

SF–Signal Frame

4 SIGNALING PROTOCOL

As previously described, at each station is assigned a unique receive time slot, which is the same as the address of the station in the logical ring of the established network. In contrast, the time slot where a station transmits its voice data is variable and it is actually the unique address (time slot) of the receiving station. In this way the calling and the called station exchange information simultaneously. As the information about the activity (status) of the stations changes with time, it is circulated by the HDLC information fields of signaling frames and is renewed as soon as it changes *ie* a station hangs up or initiates a call. Each station can communicate with another all the time but it can transmit signaling information only during the time it holds the token.

5 HARDWARE IMPLEMENTATION

The hardware is actually the electronic interface of an analog telephone set to a common bus which is shared among the users of the system. Although further details are not given here, this bus can be the power grid of a building or any other two-wire existing infrastructure. Figure 5 shows how the sets are connected to this Time Division Multiplexed bus. Each phone is interfaced using common (commercial) chips like the Subscriber Line Interface Circuit (SLIC) and PCM-COMBO chips. The PCM-COMBO states for the Combined PCM Coder and Filter, which is optimized for digital switching applications on subscriber line [3]. These chips and the associated hardware, interface to the analog telephone set and also provide the A/D and D/A conversion. This is shown in Figure 6.

The HDLC protocol runs on a specialized communications processor [5,6]. This processor is of the type of Integrated Multiprotocol Processor - IMP MOTOROLA MC68LC302, which accommodates a 68000 core and a Communications Processor (CP). The last one incorporates a main RISC controller and two serial communication controllers, which implement various protocols. Among them is the HDLC protocol, which is adopted for this application.

Each station collects from the two-wire bus the 8-bit equivalent of the analog voice samples from the other subscriber's station. The system is designed according to the European E1 multiplexing hierarchy (2.048 Mbps). According to this standard 30 time slots are used for voice traffic, one (the 16th) for the formation of the S-channel and the first (No 0) for synchronization purposes. In this system all the stations can operate either as Master Stations or Normal Stations. As described in Access to the Medium paragraph, the first station that is connected to the bus configures itself as Master Station. Any following stations are automatically identified as Normal Stations. The Master Station continuously transmits at the first time slot (No 0) an 8-bit flag (10011100). All the active stations recognize this flag and the 2.048 MHz clock is extracted in conjunction with the framing synchronization as will be described later.

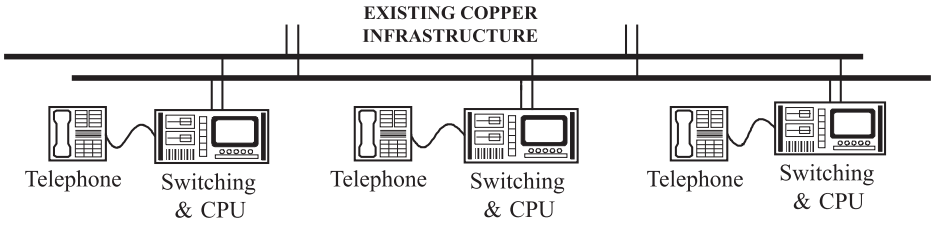

Fig. 5. Telephone sets are interfaced through custom hardware to an existing bus *eg* power line)".

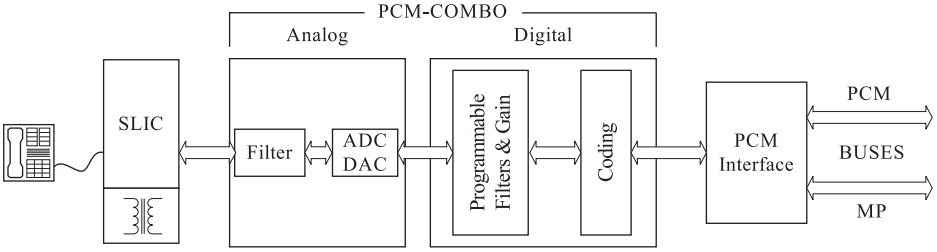

Fig. 6. SLIC/PCM-COMBO interface of the analogue phone"

Synchronization

One of the basic problems during the development was the synchronization recovery, as this was one function that was not supported by the PCM-COMBO or SLIC stages. The synchronization stage was developed in two Programmable Logic Devices (PLDs) and a Digital Phase Locked Loop (DPLL). The first PLD functions only when a station operates as Master and inserts the synchronization flag in the PCM stream. The other PLD functions in cooperation with the DPLL as a synchronization recovery stage. The Master Station incorporates a clock of 2.048 MHz. This clock drives all the other circuitry including the processor, the PCM-COMBO device and the PLD. The latter develops synchronization pulses for the processor (L1SYNC) in order to specify the time slot in which the data are transmitted and for the PCM-COMBO device (FSXR) where it specifies the beginning of the frame.

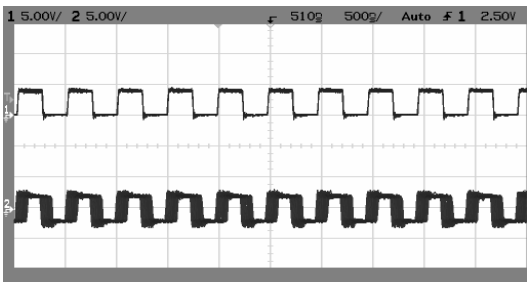

Fig. 7. Comparison between the master and extracted clock

The PCM stream is passed to the input of the DPLL device. This device incorporates two phase detectors, one of EXOR-gate type and another edge controlled phase detector (ECPD). Both detectors are combined in a ripple cancellation scheme. The PLD is incorporated in the loop, as this device implements the feedback frequency divider. In Fig. 7 the recovered clock of 2.048 MHz is shown. The jitter observed does not bother the operation of the circuit. The PCM stream also enters to an 8-bit digital comparator (contained also in the PLD). This device driven by the recovered clock seeks for the synchronization flag. When the flag is detected, an associated pulse resets all the stages that are included in the PLD. The same device produces also pulse streams for the frame synchronization of the PCM-COMBO device (FSXR) and the time slot synchronization of the microprocessor (L1SYNC) when it operates in the Normal Station mode.

Interoperability of Master and Normal Stations

In Fig. 8 it is shown the full cooperation of a Master and a Normal station by presenting the hardware parts involved from each mode of operation. It is also shown the way that both stations are connected at the two-wire bus. As referred previously, each PCM-COMBO device interfaces the microcontroller to the SLIC device. The latter is responsible for the interfacing to the telephone. Although more connections between the upper (Master) and the lower (Normal) parts are shown, the associated signals access the bus via tri-state devices. Actually there is only one physical access point to the bus from either side. In this Figure is also shown a Dual Tone Multifrequency Decoder which decodes the keypad of the analog telephone set and passes this information to the microcontroller.

6 CALL SETUP

The actual procedure for a call set-up is given in Figure 9. Initially an idle phase (on-hook) of the station is considered. The processor of the station periodically checks the off-hook detector of the SLIC module via a specific register of the PCM-COMBO module. When an off-hook state is detected the decoding of the DTMF tones is initiated. This decoding specifies the called station. If the called station is already connected to the ring (according to the internal Matrix of Connected Stations) then the information collected is stored in the processor's memory and it is transferred in the receiver address field of the HDLC protocol. A specific signaling packet (Connection Request, CREQ) is broadcasted to the ring the next time that the sending station holds the token. Every station in the ring checks if the receiver-address field of the broadcasted packet contains its unique address. If this is the case, the station processes the information field of the packet and extracts the sender address, *ie* the time slot where the called station must put its data (digitized voice) after the full establishment of the call. If the called station is not busy, a Response Frame is broadcasted using the same procedure of frame synthesis."

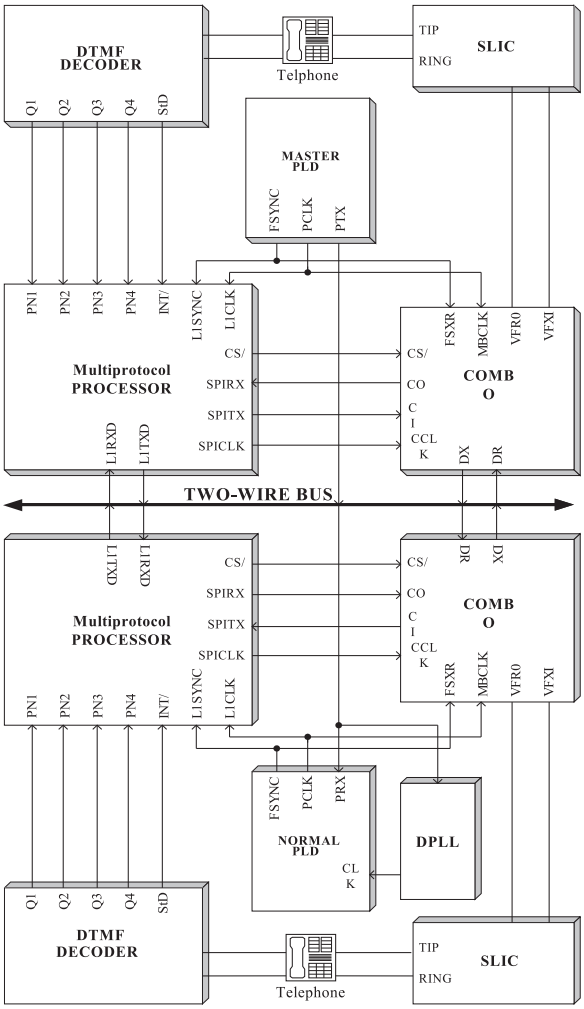

Fig. 8. Interconnection between Master and Normal station. The bold line in the middle represents the two-wire bus".

Response Frame is broadcasted using the same procedure of frame synthesis. The caller station acknowledges the response and the called station checks the state of the hook of the associated analog phone. When an off-hook state is detected at the called station a Connection Confirmation (CCON) frame is broadcasted. At this point the call has been set-up. Each processor instructs the associated PCM-COMBO module about the transmit time slot of the present connection and the two stations exchange digitized voice samples at the proper time slots. Other procedures regarding ringing and auxiliary functions also take place, but details will not be given here.

When any of the two parties hangs-up, a Disconnection Request (DREQ) frame is broadcasted. Both stations release the associated transmit time slots and return to the idle mode.

7 EXPERIMENTAL RESULTS

The whole design has been developed in an experimental basis in two sets of boards. These sets were interconnected via two wires and one of the boards was configured as Master while the other was configured as Normal station. The two sets were functioning properly and the allocation of the voice information to any time slot was possible. The observed voice quality was at the expected level that is provided when no compression is used (64 Kbps).

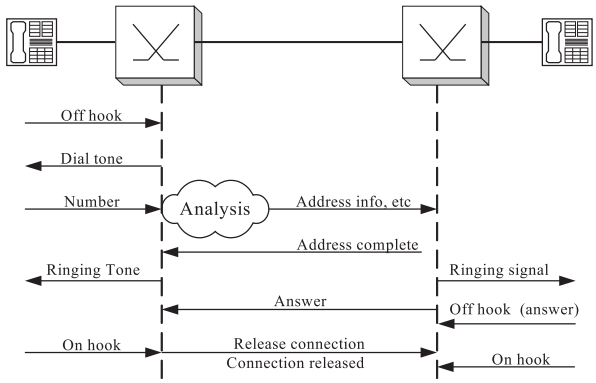

Fig. 9. Procedures for the set-up and release of a telephone call

In the following figures we present some experimental results of the bus traffic. In the bottom half of Fig. 10 (using the zoom function of the oscilloscope), data transmitted on the line are shown. For demonstration purposes, only six of the 32 time slots of a PCM frame where used. As displayed, a sync pulse is ahead of the first time slot (*ie* the flag 10011100), to denote the start of the frame. After that, two time slots which carry digital voice data follow, utilized by two subscribers during that time. Then, follow two time slots that are not seized at the moment,

and next the time slot used for exchanging signaling data between the stations appears. In the above example, time slot No 6 is handled instead of the 16-th.

The data being transmitted on the signaling (S) channel are shown in Fig. 11 (2nd and 4th traces). A synchronization pulse precedes as shown at the upper and 3rd traces. Bottom half of the image is a zoomed version of the above. It is shown that the microprocessor can receive and transmit data on the medium, only when a specific sync pulse appears on its time slot assignment pin. As stated above, the processor will exploit as many time slots as it is required to transmit a whole HDLC frame, when the station has the permission to transmit signaling data.

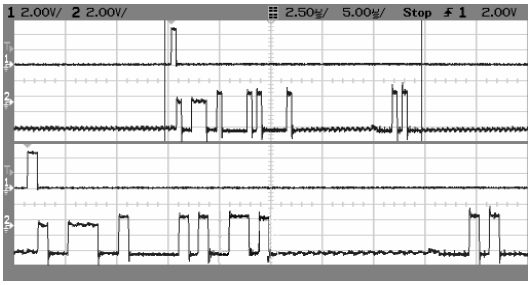

Fig. 10. Frame synchronization pulse (upper trace) and data transmitted on the bus (second trace). Bottom traces is the magnification of the upper.

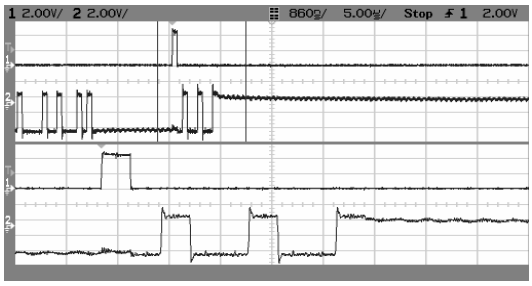

Fig. 11. Data transmitted by the processor during time slot No 6 and the sync pulse for choosing internal channel. Upper trace: Synchronization pulse that identifies the time slot of the S-channel. Second trace: data on the S-channel (HDLC protocol). Lower traces are the magnification of the above.

8 CONCLUSIONS

In this paper a switching technique for voice traffic is reported. The technique is applicable when no special telephone cabling is available. The switching function is distributed to all stations involved, so only a two-wire bus is sufficient for their parallel interconnection. For this bus the power lines of a building can be used. We present block diagrams of the hardware and flow diagrams of the software of the associated microcontroller. The experiments conducted, confirmed the operation and efficiency of the whole system. One Master and one Normal station were utilized, making use of the frame synchronization and clock recovery methods recommended. The telephone call setup and release functions adopt the HDLC protocol. Tests that were carried out verified the ability of the system to manage both digital voice data corresponding to telephone call connections and control messages exchanged by the microprocessors.

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