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FEEDBACK CONTROL OF DC LINK VOLTAGE OF THE BACK–TO–BACK PWM MULTILEVEL CONVERTER

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A serious constraint in a multilevel inverter is the capacitor voltage-balancing problem. The unbalance of the different DC voltage sources of the nine-level neutral point clamping (NPC) voltage source inverter (VSI) constituted the major limitation for the uses of this new power converter. In order to stabilize these DC voltages, we propose in this paper to study the cascade constituted by three phases three-level PWM rectifier-clamping bridge filter-nine-level NPC voltage source inverter (VSI). In the first part, the authors present a topology of nine-level NPC, and then they propose a model of this converter and the algebraic PWM strategy to control it. Then in the second part we study the three-level PWM rectifier controlled by hysteresis strategy. In the last part of this paper, the authors study the stability problem of the input DC voltages of the inverter. To remedy to this problem, the authors propose a solution which uses a feedback control for this cascade. The results obtained are full of promise to use the inverter in high voltage and great power applications as electrical traction.

K e y w o r d s: NPC inverter, clamping bridge, rectifier multilevel, current hysteresis, PWM strategy, input DC voltages, power factor unit, regulation

1 INTRODUCTION

The variable speed control of electrical machines has great advantages in the industrial processes. Mainly, it improves their static and dynamic performances. The apparition of new power components controllable in the opened and closed (GTO and IGBT) has led to the conception of new and fast converters for high power applications. In this paper, we develop a new multilevel source inverter: nine-level NPC VSI used in high voltage and great power applications, [1].

In the first part, they develop knowledge and a control model of this converter, [2,3]. In the second part, the authors propose a PWM strategy which uses eight bipolar carriers. As application, we study the performances of the speed control of PMSM fed by this inverter, [4,5]. In this part, the authors use constant input DC voltages [7, 8, 9].

In the last part of this paper, the authors study the stability problem of the input DC voltages source inverter. Thus, they study a cascade constituted by three-level PWM rectifier-clamping bridge-filter-nine-level NPC VSI [4,6]. This study shows the effect of the stability problem of the DC voltages on the PMSM performances. To remedy to this problem, the authors propose a solution which uses feedback control for this cascade [1,4]. The results obtained confirm the good performances of the proposed solution.

2 MODELLING AND CONTROL OF NINE–LEVEL NPC VSI

The three phases nine levels NPC VSI is a new structure of power conversion used to feed with variable frequency and voltage, a great power alternative current machine. Several structures are possible for nine level inverters. In this paper we study the neutral point clamping structure (Fig. 1). This structure is constituted by three arms and eight DC voltages sources. Every arm has sixteen bi-directional switches, ten in series and six in parallel and two diodes DD_{i0} and DD_{i1} Which let to have zero voltage for V_{KM} (V_{KM} is the voltage of the phase K relatively to the middle point M) [1, 2].

Several complementary laws are possible for nine-level NPC VSI. The optimal complementary law used for this converter is presented below:

$$\begin{aligned} &B_{i6} = \overline{B}_{i2}\,, \qquad B_{i7} = \overline{B}_{i1}\,, \qquad B_{i8} = \overline{B}_{i3}\,, \\ &B_{i9} = B_{i4}\,, \qquad B_{i10} = \overline{B}_{i5}\,. \end{aligned} \tag{1}$$

B_{is}: control signal of the semiconductor TD_{is}

2.1 Knowledge model of nine-level NPC VSI

In a controllable mode using the proposed complementary law, we define for each semi- conductor TD_{is} a connection function F_{is} as fellow [1, 3]:

$$F_{is} = \begin{cases} i & \text{if } TD_{is} \text{ is closed,} \\ 0 & \text{if } TD_{is} \text{ is open.} \end{cases} \tag{2}$$

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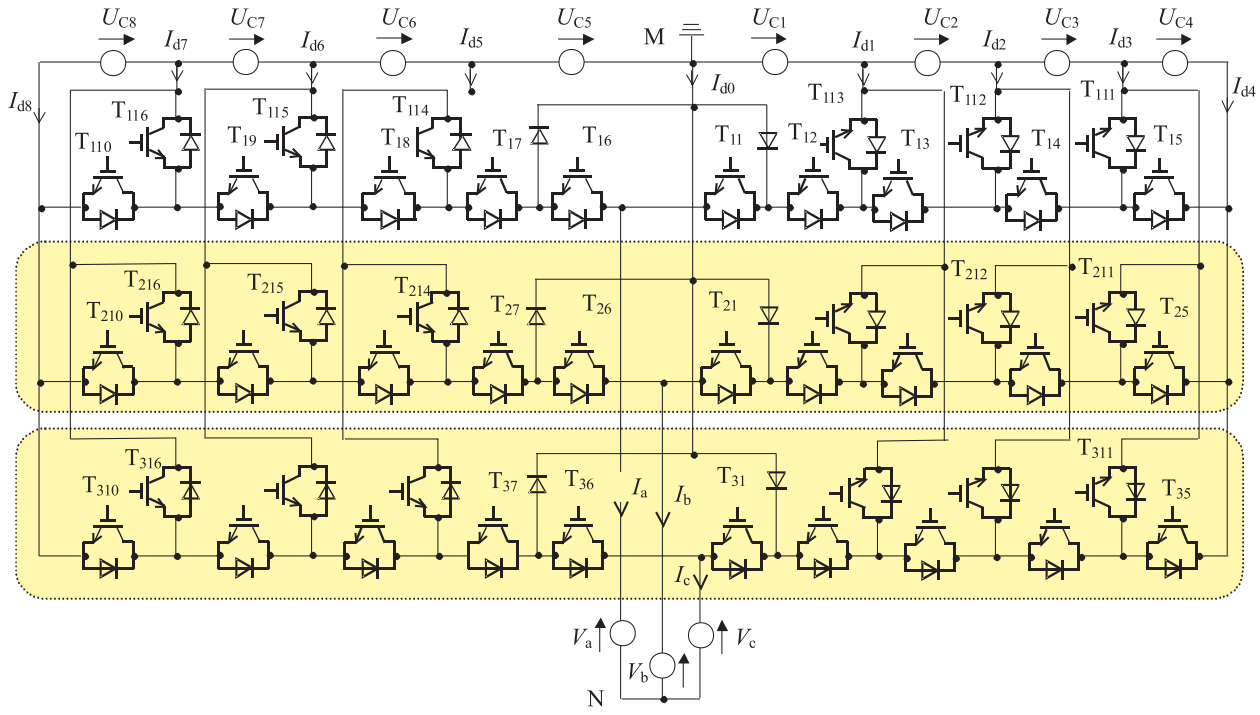

Fig. 1. Three-phase nine-level NPC VSI configuration

(i: number of the arms and s: number of the semiconductors).

The input voltage of the inverter, relatively to the middle point M, is given by the following system:

$$\begin{aligned}V_{KM} = {} & F_{i1}F_{i2}(1-F_{i3})U_{C1} + F_{i1}F_{i2}F_{i3}(1-F_{i4})(U_{C1}+U_{C2}) \\ & + F_{i1}F_{i2}F_{i3}F_{i4}(1-F_{i5})(U_{C1}+U_{C2}+U_{C3}) \\ & + F_{i1}F_{i2}F_{i3}F_{i4}F_{i5}(U_{C1}+U_{C2}+U_{C3}+U_{C4}) \\ & - F_{i6}F_{i7}(1-F_{i8})U_{C5} - F_{i6}F_{i7}F_{i8}(1-F_{i9})(U_{C5}+U_{C6}) \\ & - F_{i6}F_{i7}F_{i8}F_{i9}(1-F_{i10})(U_{C5}+U_{C6}+U_{C7}) \\ & - F_{i6}F_{i7}F_{i8}F_{i9}F_{i10}(U_{C5}+U_{C6}+U_{C7}+U_{C8}) \end{aligned} \quad (3)$$

where $K \in \{A, B, C\}$ and respectively $i \in \{1, 2, 3\}$.

In order to reduce the above equation and define a control model of the converter, we define the half arm connection function F_{i1}^b and F_{i0}^b associated respectively to the upper and lower half arms.

$$\begin{aligned} F_{i1}^b &= F_{i11}F_{i12}F_{i13}F_{i14}F_{i15}\,, \\ F_{i0}^b &= F_{i16}F_{i17}F_{i18}F_{i9}F_{i110}\,. \end{aligned} \quad (4)$$

We suppose: $Uc_{i(i=1\div 8)} = Uc$. We note that:

$$\begin{bmatrix} V_{AM} \\ V_{BM} \\ V_{CM} \end{bmatrix} = \begin{bmatrix} 3F_{111} + 2F_{112} + 4F_{11}^b + F_{113} - F_{114} - \\ \qquad 2F_{115} - 3F_{116} - 4F_{10}^b \\ 3F_{211} + 2F_{212} + 4F_{21}^b + F_{213} - F_{214} - \\ \qquad 2F_{215} - 3F_{216} - 4F_{20}^b \\ 3F_{311} + 2F_{312} + 4F_{31}^b + F_{313} - F_{314} - \\ \qquad 2F_{315} - 3F_{316} - 4F_{30}^b \end{bmatrix} U_C\,. \quad (5)$$

The system (5) shows that a nine-level NPC VSI is equivalent to eight two-level or four three-level or two five-level NPC VSI in series.

For the equation (5), we define a global half arm connection function:

$$\begin{aligned} F_{i1}^{b\top} &= F_{i13} + 2F_{i12} + 3F_{i11} + 4F_{i11}^b\,, \\ F_{i0}^{b\top} &= F_{i14} + 2F_{i15} + 3F_{i16} + 4F_{i10}^b\,. \end{aligned} \quad (6)$$

When $F_{i1}^{b\top}$ equal to 0, the upper half arm is open, and if $F_{i1}^{b\top}$ equal to 0, the lower half arm is open too. The simple voltages of three phases nine-level NPC VSI are given by the following system:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} F_{11}^{b\top} - F_{10}^{b\top} \\ F_{21}^{b\top} - F_{20}^{b\top} \\ F_{31}^{b\top} - F_{30}^{b\top} \end{bmatrix} U_C\,. \quad (7)$$

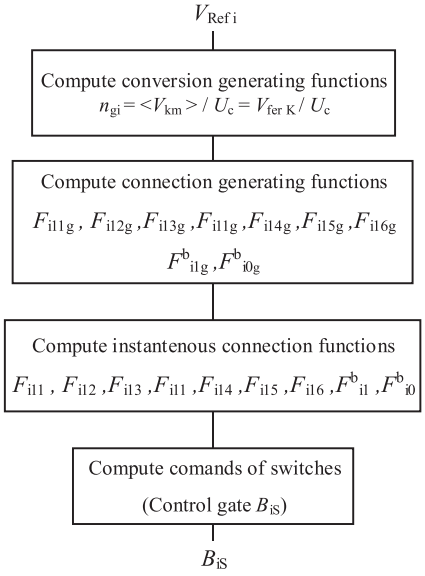

Fig. 2. The general of flow chart of an algebraic modulation using the control model of nine-level NPC VSI

2.2 Control model of nine-level NPC VSI

The model established above is discontinuous. It is used to simulate PWM strategies. In order to develop a control model of this inverter, we define the average model of the knowledge one. Thus, we define the generating function "X_g" of a discontinuous one "X", as the mean value of "X" on a modulation period "T_m" supposed very small as follow [5, 6]:

$$X_g = \frac{1}{T_m} \int_0^{T_m} x \mathrm{d}t \,. \tag{8}$$

The control model of three phases nine-level NPC VSI, deduced from the system (8), is given by the following equation where $\langle V_A \rangle$, $\langle V_B \rangle$ and $\langle V_C \rangle$ represent the mean value of the instantaneous ones.

$$\begin{bmatrix} \langle V_A \rangle \\ \langle V_B \rangle \\ \langle V_C \rangle \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} (F_{11}^{b\top})_g - (F_{10}^{b\top})_g \\ (F_{21}^{b\top})_g - (F_{20}^{b\top})_g \\ (F_{31}^{b\top})_g - (F_{30}^{b\top})_g \end{bmatrix} U_C \tag{9}$$

with:

$$\begin{aligned} \left(F_{i1}^{b\top}\right)_g &= \left(F_{i13}\right)_g + 2\left(F_{i14}\right)_g + 3\left(F_{i15}\right)_g + 4\left(F_{i11}\right)_g \,, \\ \left(F_{i0}^{b\top}\right)_g &= \left(F_{i14}\right)_g + 2\left(F_{i15}\right)_g + 3\left(F_{i16}\right)_g + 4\left(F_{i10}\right)_g \,. \end{aligned} \tag{10}$$

2.3 Algebraic PWM strategies of nine-level NPC VSI

The different triangular-sinusoidal strategies can be archived with digital mean by sampling reference voltage $V_{\text{ref}i}$ such as $V_{\text{ref}i} = V_{\text{ref}}\sqrt{2}\sin\left(\omega i - \frac{2}{3}\pi(i-1)\right)$. In this paper, we develop a digital PWM algorithm of nine-level NPC VSI destined for a digital realisation and developed using the control model elaborated previously [2, 4]. The general flow chart of an algebraic PWM using this control model is presented in Fig. 2. This strategies is characterized by modulation index (m) defined as ratio between the frequency f_p of the carrier and the frequency of the reference voltage $\left(m = \frac{f_p}{f}\right)$, and modulation rate (r) is the ratio between the magnitude V_{KM} of the reference voltage of the reference voltage and four times of the carrier magnitude $\left(r = \frac{V_m}{4U_{pm}}\right)$.

Figure 3 represents the simple output voltage of nine-level NPC VSI controlled by the proposed algebraic modulation for $m = 36$, 39 and $r = 0.9$. We notice that:

- If m is even, the simple output voltage has a symmetry relatively to $\frac{\pi}{2}$ and π. So we have only the odd harmonics.
- If m is odd, we have no symmetry and then all harmonics exist.

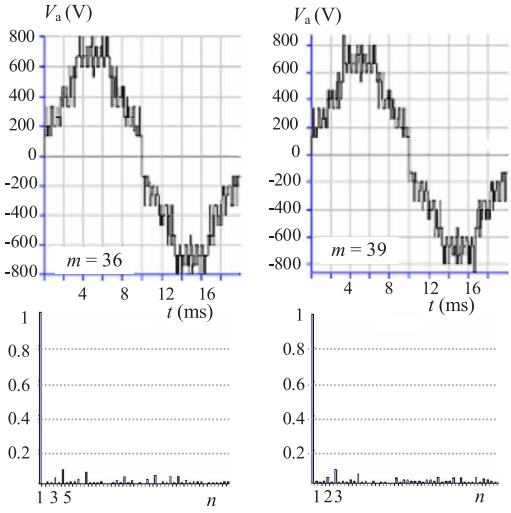

Fig. 3. The simple voltage of the inverter and its spectrum

The voltage harmonics gather by families centred around frequencies multiple of mf (Fig. 3). The first family centred around mf is the most important in view of its magnitude.

3 THREE–LEVEL PWM RECTIFIER–CLAMPING BRIDGE–FILTER–NINE–LEVEL NPC VSI–PMSM CASCADE

In this part, we study a generation input DC voltages manner. For these we propose a cascade presented in Fig. 4.

3.1 Modelling of three-level PWM rectifier:

The advantages of three-Level Voltage Source Inverter topology (Fig. 5) are well known and have been applied in medium and high power applications in the last years

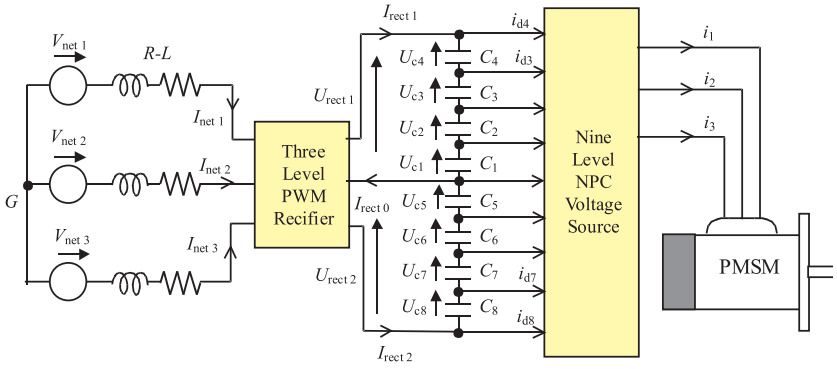

Fig. 4. Three level PWM rectifier-clamping bridge-filter-nine-level NPC VSI-PMSM cascade

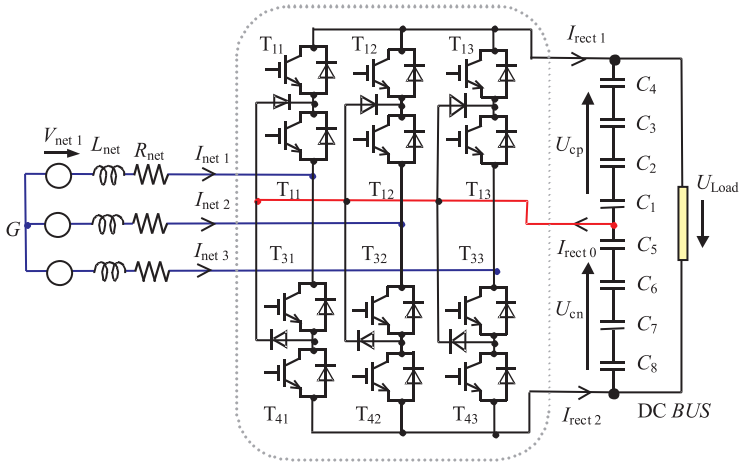

Fig. 5. Three-level VSI inverter topology

[3, 4]. The reduction of switching frequency and the increment of the voltage supported by each device are very attractive features.

The reversibility of three-level source inverter allows it to work as current rectifier [2, 10]. This optimal control of this rectifier is:

$$B_{i3} = \overline{B}_{i2}\,, \qquad B_{i4} = \overline{B}_{i1} \tag{11}$$

with $i \in, 2, 3\}$

The input voltages of three-level PWM rectifier are defined as follows:

$$\begin{bmatrix} V^A \\ V^B \\ V^C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left\{ \begin{bmatrix} F^b_{11} \\ F^b_{21} \\ F^b_{31} \end{bmatrix} U_{\text{rect1}} - \begin{bmatrix} F^b_{10} \\ F^b_{20} \\ F^b_{30} \end{bmatrix} U_{\text{rect2}} \right\} \tag{12}$$

The rectifier output current is given as follows:

$$\begin{aligned} i_{\text{rect1}} &= F^b_{11} i_{\text{net1}} + F^b_{21} i_{\text{net2}} + F^b_{31} i_{\text{net3}} \\ i_{\text{rect2}} &= F^b_{10} i_{\text{net1}} + F^b_{20} i_{\text{net2}} + F^b_{30} i_{\text{net3}} \end{aligned} \tag{13}$$

With $i_{\text{rect0}} = -\big(i_{\text{rect1}} + i_{\text{rect2}}\big)$

3.2 Double hysteresis-band current control

The basic principle of the double hysteresis- band current control is based on the classical hysteresis control applied to conventional two-level inverters. Who we define two hysteresis bands (Upper and Lower Commutation Bands) around the current reference value [3, 4, 10]. The hysteresis bands are actually superimposed but to differentiate them, they will be named as Upper and Lower band. The band change could be obtained by means of a simple logic circuit when using two slightly shifted bands [3, 4, 8]. However, to avoid the influence of noise, this option was rejected. Its algorithm is given by Fig. 6 [4].

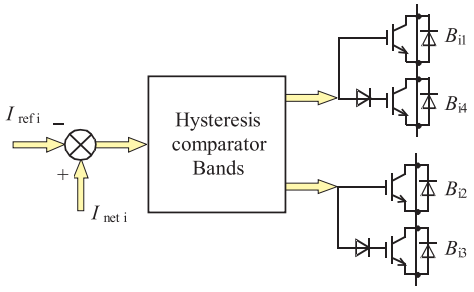

Fig. 6. Principle of the hysteresis control

$\mathcal{E}_i$ is the difference between reference current $I_{\text{ref}i}$ and real current $I_{\text{net}i}$:

$$\varepsilon_i = I_{\text{net}i} - I_{\text{ref}i}\,, \tag{14}$$

$$\begin{aligned}
&[(\varepsilon_i \geqslant \Delta h)\&(\varepsilon_i \leqslant 2\Delta h)]\,\text{Or}\,[(\varepsilon_i \leqslant -\Delta h)\&(\varepsilon_i \geqslant -2\Delta h)] \\
&\qquad \Rightarrow B_{i1} = 1\,, B_{i2} = 0 \\
&\qquad (\varepsilon_i < -2\Delta h) \Rightarrow B_{i1} = 0\,, B_{i2} = 0 \\
&\qquad (\varepsilon_i < -2h) \Rightarrow B_{i1} = 1\,, B_{i2} = 1\,.
\end{aligned} \tag{15}$$

Δh: hysteresis band width.

3.3 Modelling and control of clamping bridge

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series connected in parallel with capacitor as shown in Fig. 7. The transistors are controlled in order to maintain an equality of the different voltages.

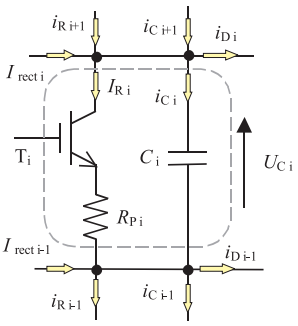

Fig. 7. The clamping bridge cell

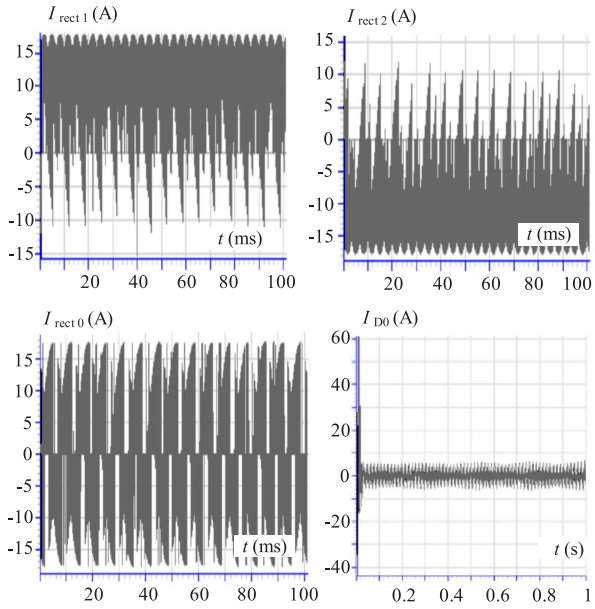

Fig. 8. The input and output currents of the rectifier current $I_{\text{rect}\,i}$ and I_{D0} of nine-level NPC VSI

In this part, the model of intermediate filter with clamping bridge is defined by following equation:

$$C_i \frac{\mathrm{d}Uc_i}{\mathrm{d}t} = \text{Irect}_i + \text{ir}_{(i+1)} + \text{ic}_{(i+1)} - \text{id}_i - \text{ir}_i \tag{16}$$

with

$$\text{ir}_i = T_i \frac{Uc_i}{Rp_i}\,. \tag{17}$$

Figures 8 and 9 show the simulation results to use the clamping bridge. We observe the input and output currents of the rectifier current $i_{\text{rect}i}$, i_{d0} of nine-level NPC VSI (Fig. 8). The currents $i_{\text{rect}1}$ is the opposite of the current $i_{\text{rect}2}$. The current $i_{\text{rect}0}$ and i_{d0} have a mean value practically zero.

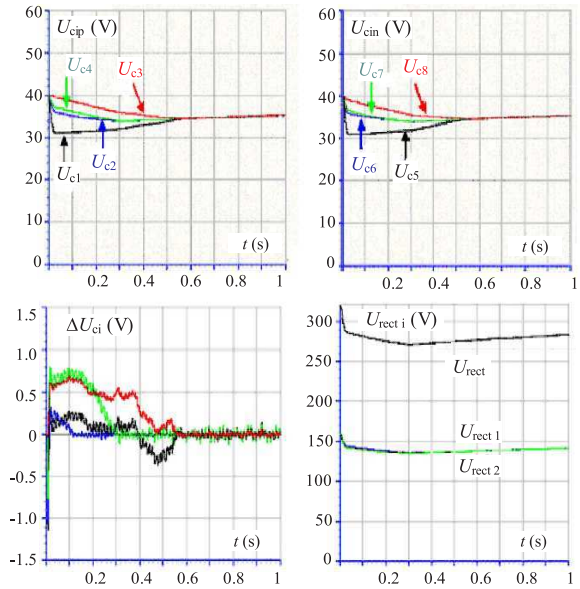

Fig. 9. The different input DC voltage source and the output DC voltages of three-level PWM rectifier

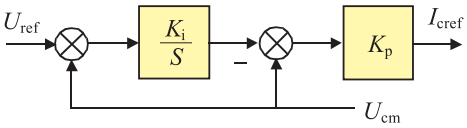

Fig. 10. Integrator proportional regulator structure

In Fig 9 we show the performances of the bridge clamping control of the output voltage of the PWM rectifier. We note that, the output voltage of PWM rectifier is constant. Therefore the different input DC voltages of the nine-level NPC VSI are constant and practically equal by pairs too. ($U_{C1} = U_{C5}$, $U_{C2} = U_{C6}$, $U_{C3} = U_{C7}$ and $U_{C4} = U_{C8}$). The difference of the input voltages of nine-level NPC inverter is decrease to have a value practically null in steady states, and this difference is equal zero (Fig. 9). The different of the output DC voltages of three-level NPC rectifier $U_{\text{rect}i}$ is decrease (is not constant) (Fig. 9).

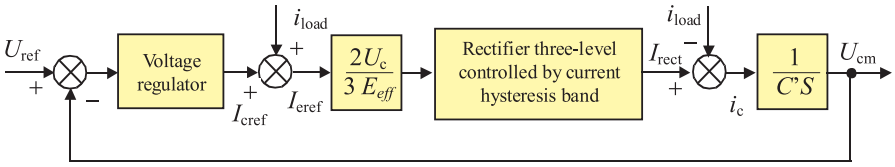

Fig. 11. Feedback control of the output voltage of three-level rectifier

4 FEEDBACK CONTROL OF THREE–LEVEL PWM RECTIFIER

To remedy to the problem of the instability of the output DC voltage of PWM rectifier [7, 8, 9], we propose to enslave it using integrator-proportional regulator as shown in Fig. 10.

We use a regulator IP for voltage, the general principle enslavement of three-level rectifier is given by Fig. 11.

We have observe then the application of the enslavement algorithm for a cascade constituted by three levels PWM rectifier-clamping bridge-nine levels NPC VSI. Figure 12 shows the performances of the feedback control of the output voltage of three-level PWM rectifier. We remark that the network currents i_{neti} feeding rectifier follow perfectly their sinusoidal references (Fig. 12).The network voltage and current are in phases then the power factor of network is uniting (Fig. 12).

We note that, the output voltage of PWM rectifier follows perfectly its reference which is constant (Fig. 13).

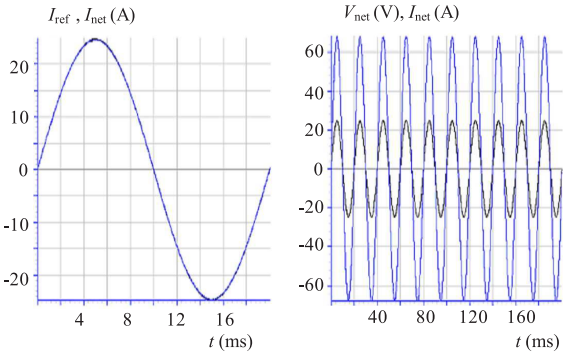

Fig. 12. The network current I_{net} , its reference I_{ref} and its voltage V_{netr}

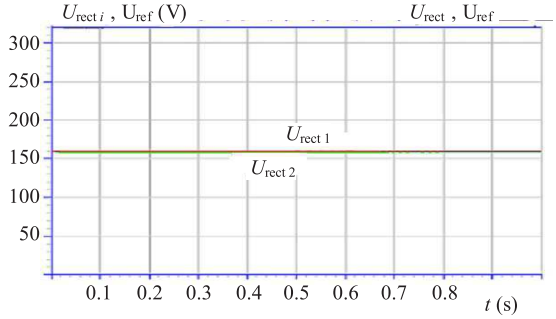

Fig. 13. The output DC voltages of three-level PWM rectifier

5 PERMANENT MAGNET SYNCHRONOUS MACHINE DRIVE

5.1 Permanent magnet synchronous machine (PMSM) modelling

The Park model of the permanent magnet synchronous machine, with P pairs of poles, is defined by the following equations system [11].

$$\begin{bmatrix} V_{ds} \\ V_{qs} \end{bmatrix} = \begin{bmatrix} R & -L_q\omega \\ L_d\omega & R \end{bmatrix} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \omega\Phi_f \begin{bmatrix} 0 \\ 1 \end{bmatrix}. \quad (18)$$

The electromagnetic torque is given by the following expression.

$$T_{em} = P\left[\Phi_d I_{qs} - \Phi_q I_{ds}\right] = P\left[\left(L_d - L_q\right) I_{ds} + \Phi_f\right] I_{qs}\,. \quad (19)$$

5.2 Vector control of the PMSM

The control strategy often used consists to maintain the current i_{ds} to zero, and to control the speed by the current i_{qs} via the voltage V_{qs}. When the current i_{ds} is zero, the PMSM model presented in figure 14 is reduced, for the axis q, to separately excitation DC machine equivalent. Regulate the current i_{ds} to zero lets have, for a given stator currents magnitude, a maximum torque. In this paper, we use the algorithm $i_{ds} = 0$ (Fig. 15) [11, 12].

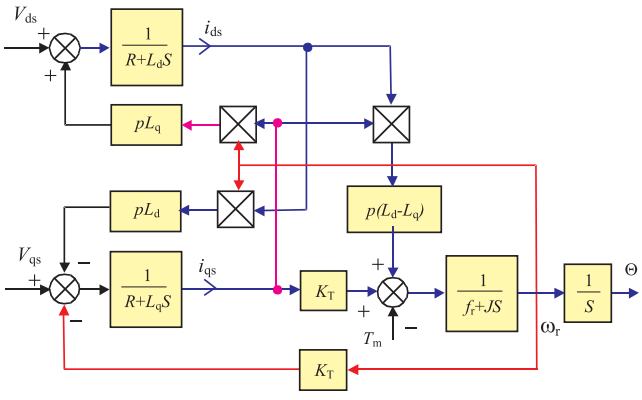

Fig. 14. The model of the PMSM

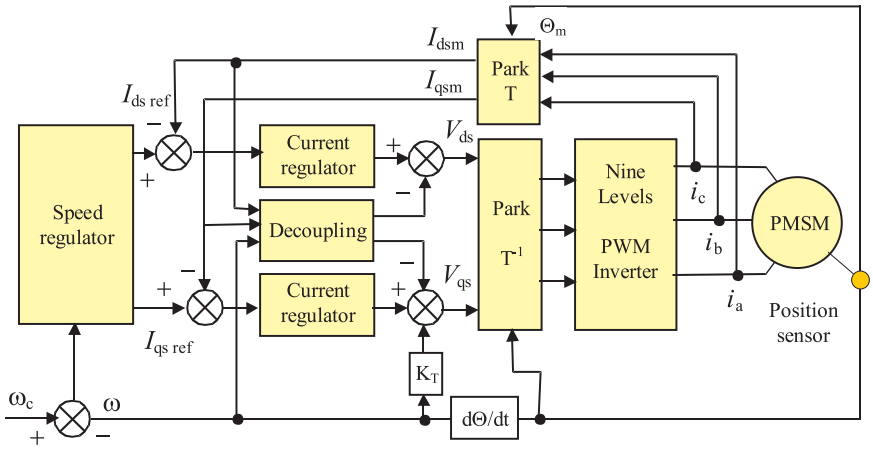

Fig. 15. Speed control using the algorithm $i_{ds} = 0$

5.3 Speed control of PMSM fed by nine levels NPC VSI

In this part, we will study the performances of the speed control of PMSM fed by nine- level NPC inverter controlled by the proposed algebraic PWM strategies.

The PMSM is drive using vector control with direct current reference null. Figure 16 shows the current i_{ds} is practically null, the speed follows quietly its reference, and the current i_{qs} and the torque are practically proportional

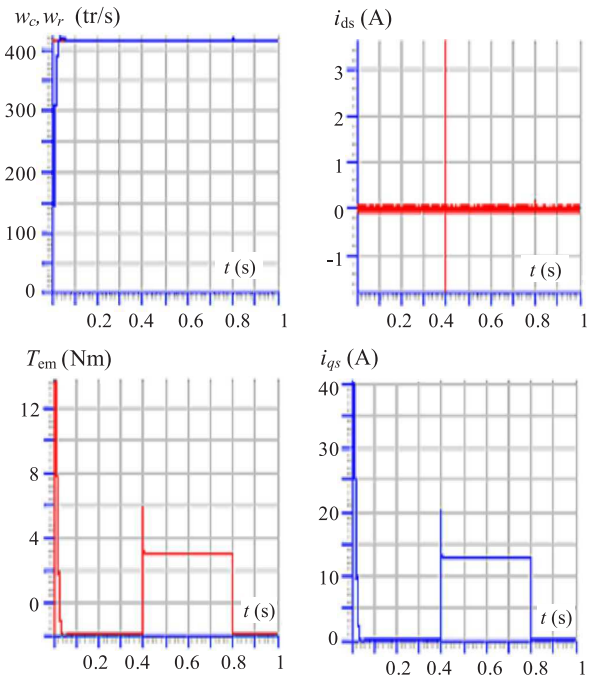

Fig. 16. PMSM performances fed by nine-level NPC inverter Cascade

6 CONCLUSION

In this paper, we have studied stability problem of the input voltage of the nine-level NPC inverter. The study of the stability problem of the input voltages of nine-level NPC inverter using a cascade constituted by three-level PWM rectifier-Clamping bridge- filter-nine-level NPC VSI.

The application of the linear feedback shows parfait following of the output of rectifier and his reference and the stability of the input voltage of nine-level NPC inverter. have shows is possible to conceiver, with frequency charger using in output the nine- level inverter, PMSM variator with feeble rate of harmonics, a power factor of network unity and great charge dynamics performance.

This study shows the effect of the stability of the DC voltages on the PMSM performances. The results obtained with this solution confirm the good performances and full promise to use the inverter in high voltage and great power applications as electrical traction.

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