Journal of ELECTRICAL ENGINEERING, VOL. 59, NO. 6, 2008, 332–338

REVIEWS - LETTERS - REPORTS

OPTIMUM VIAS DISTRIBUTION TO A PRINTED CIRCUIT BOARD

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Nowadays because of impressive development of power electronic components and integrated circuits there is a high density of active electronic components on printed circuit boards (PCB). This also had involved new aspects as regards the thermal power management at the contact between the power semiconductor case and the printed circuit board. So, a multi-layers PCB and vias solution have been adopted to improve the thermal exchange between the power components and environment. At a given density of active electronic components it is important to achieve an optimum vias distribution on the PCB. 3D thermal simulations have been used in order to analyze the vias distribution and its geometry on the basis of the thermal resistance principle.

K e y w o r d s: printed circuit board, vias distribution, thermal analysis

1 INTRODUCTION

In less than 35 years, since the first power MOSFET was introduced, the use of power electronics for both industrial and commercial applications has been increasing exponentially. In fact, the high input impedance of these devices allowed a considerable simplification of the control circuits cutting off costs and dimensions of power electronics systems. Furthermore, the higher switching speed of these new devices allows a faster control of the energy flow improving the performances of the new converters. The intrinsic current carrying capability limitation of MOS devices has been overcome around the middle of the 80s with the introduction of the IGBT, which merged the advantages of the bipolar devices (low forward voltage drop almost independent of blocking voltage) with the ones of MOS devices (high input impedance and fast switching). The control circuit miniaturization allowed by the MOS devices opened the door to the possibility of integrating part of these circuits within the same power semiconductor package. These new characteristics open new scenarios for the power electronics industry, which is today called to invest resources in the development of more efficient and less costly power converters. This task is today of extreme importance considering that about 70 % of the total electric energy produced flows through power semiconductors.

2 THERMAL ASPECTS AS REGARDS THE PCB

Heat transfer in and around a printed circuit board (PCB) is generally very complex. Some of the heat generated in components is conducted away through the multiple conducting (trace) layers, vias, and dielectric layers of the board; and some is dissipated by convection and radiation from the exposed surfaces. In order to improve the thermal exchange between power semiconductors mounted on PCB and environment, a certain number of vias under power electronic components have been created. Vias are holes that are drilled in the board and then plated with copper to make electrical connections between traces that are on different layers of the board. Vias can be "thru" vias where they go completely through the board, "blind" vias where they enter one side and stop at an internal layer, and "buried" vias where they connect between internal layers of the board. Thermally, vias play a significant role in locally enhancing the heat conduction through the board thickness because the thermal conductivity of copper can be as much as 1200 times that of common dielectric materials.

Thermal analysis assists the designer in determining the electrical performance of the components on a PCB, and it also helps the designer to determine if the component or PCB will burn-up due to high temperatures. Thermal analysis can be as simple as the calculation of the average temperature of a PCB, or it can be as complicated as a transient model of an electronics-box with multiple PCB's and thousands of components, [1]. The steady state power limit is dependent mainly upon system level parameters such as heat sinking, cooling mode, *ie*, natural or forced convection, and PCB power loading [2]. For better use of the already available PCB material, three-dimensional component layout and flexible PCB technology are utilized to gain advantages [3–5]. There are many problems at a hybrid integrated power electronic module for medium power converter, when packaged with the power circuit closely, the driver and protection printed circuit board is affected seriously by heat generated from power chips in the power circuit [6, 7]. The solutions mean

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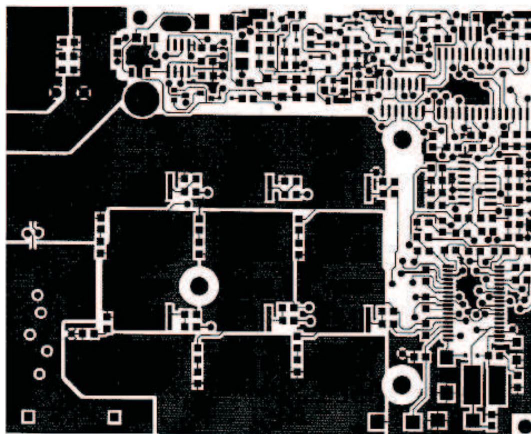

Fig. 1. Example of PCB

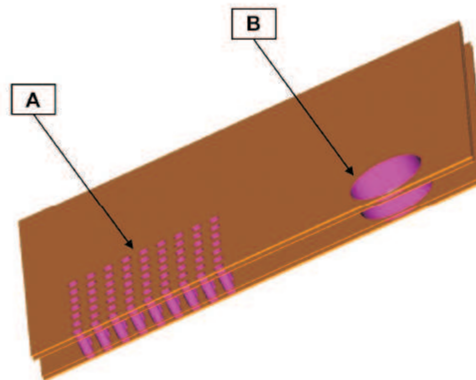

Fig. 2. 3D model used for the thermal simulation

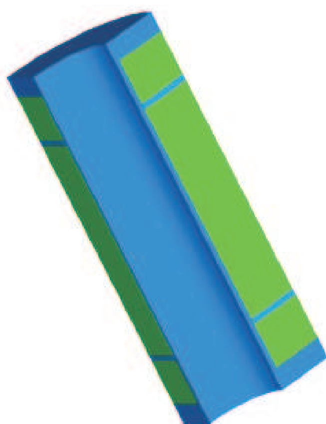

Fig. 3. 3D drawing of the vias "as it is"

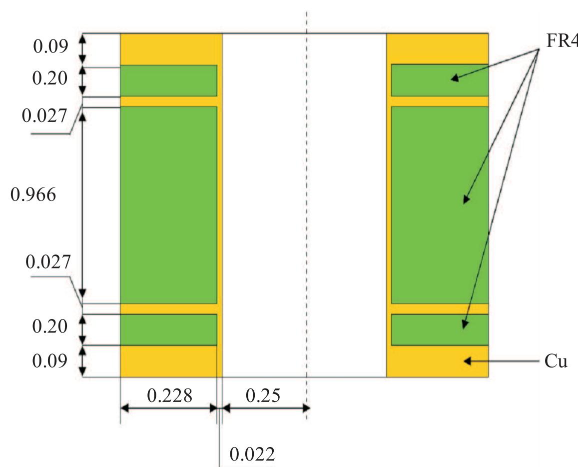

Fig. 4. Vias model dimensions

Table 1. Material properties

Properties	Copper (Cu)	Materials FR4 Epoxy Glass	New vias material
Density (g/mm^3)	8.9×10^{-3}	1.9×10^{-3}	
Specific heat (J/°Ckg)	3.85×10^2	1.15^3	
Thermal conductivity (W/°Cm)	385	0.294	85.2(62.5)

to improve the power packages thermal path [8, 9], and to increase PCB thermal conductivity and heat spreading capability by introducing an extra copper content [10], unique PCB technologies including embedded heat-sinks [11], or using a copper- alumina PCB, [12], carbon composite layer [13] or thin carbon composite laminate is used in the integral structure of PCB [14].

Approaches to simulate these processes have already been made in earlier works [15, 16]. In [17] a thermal map has been obtained of the surface temperature from which the component layout and thermal profiles can be estimated. The thermal resistance between the component fingers and the bottom surface of a multi-layer printed circuit board is computed using a finite element method (FEM) simulation [18], or a reduced 3D model based on the device's physical structure is presented in [19]. A user-friendly CAD system allowing to obtain the composite colour isotherms with the PCB photo is shown in [20]. There was developed a methodology of coupling statistical with thermal computational fluid dynamics software tool to efficiently optimize the thermal performance of PCB [21]. Also a 2D FEM analysis of PCB can be implemented in the optimization procedure for obtaining the optimal chip/component placement based on thermal constraints [22].

3 THERMAL MODEL

A complex but not uncommon example of PCB is shown in Fig. 1. This kind of PCB layout means the electric circuit of an inverter that includes some power MOSFET components.

Starting from initial PCB layout, the region nearby the current input it has been extracted, as shown in Fig. 2 below. In particular, the model includes the region between the area where the current is injected B and the copper

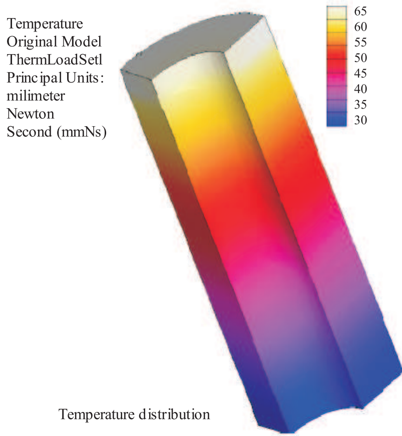

Fig. 5. Vias simulation

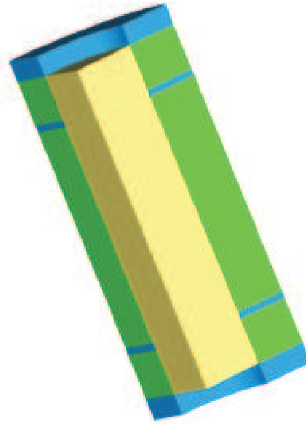

Fig. 6. Simplified thermal vias

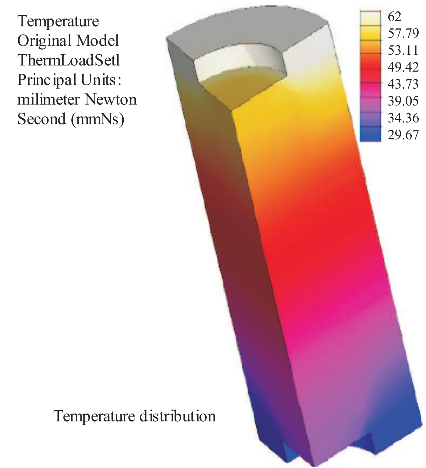

Fig. 7. Temperature distribution at the simplified vias model

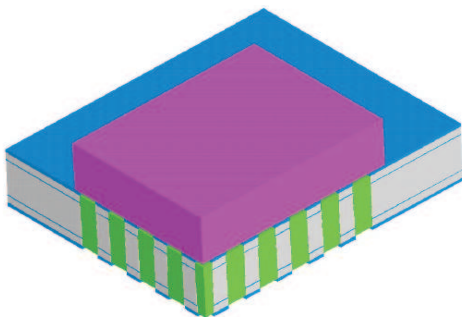

Fig. 8. Power PCB using linear distribution of vias

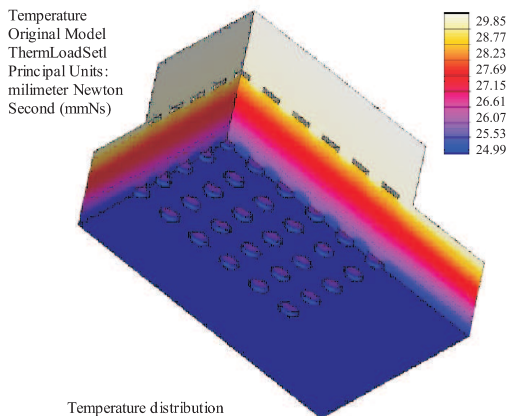

Fig. 9. Temperature values in the case of linear vias distribution

case of the first power MOSFET A. This region has been chosen since it is the one with the highest current stress. In fact, the whole load DC current flows through the copper layers of this part of the circuit.

3.1 Setup of a simplified model of the thermal vias

First of all a complete model of the thermal vias has bee analyzed. The vias geometry has been made in Pro/ENGINEER, see Fig. 3. The vias model has an internal diameter of 0.5 mm and a surrounding area of PCB to form a cylinder of 1 mm external diameter. The above model has the dimensions and materials reported in Fig. 4 and Table 1.

The above model has been simulated in the following conditions: Tbot = 25°C (temperature of the vias botom); $P = 100$ mW at quarter of vias (applied to the top surface of the vias). The result is shown in Fig. 5.

The maximum temperature is 67.15°C, so the thermal resistance is,

$$R_{th} = (67.15 - 25)/(4 * 0.1) = 105.375(°\mathrm{C/W})\,.$$

Total time of simulation: 46.30 seconds.

A simplified model of the initial thermal vias has been made, Fig. 6, using the principle of the same thermal resistance.

As it can be noticed, the internal thickness of copper has been replaced with a new material (new density and thermal conductivity). The thermal simulation in the same conditions as the initial vias is shown in Fig. 7, below.

In this case, the thermal resistance is:

$$R_{th} = (67.17 - 25)/(4 * 0.1) = 105.425(°\mathrm{C/W})$$

that is very close to the initial thermal resistance, 105.375°C/W. Furthermore, the total elapsed time for the simulation is 8.78 seconds. Thus, the new model allows reducing the simulation time by 5.27 times.

3.2 Thermal model and the simulation of the starting conditions

Taking into account the simplified model for thermal vias, two thermal models for two for two basic geometries (a linear and a diagonal distribution of vias) have been built. The following PCB characteristics have been used:

- thickness of 1.6 mm;

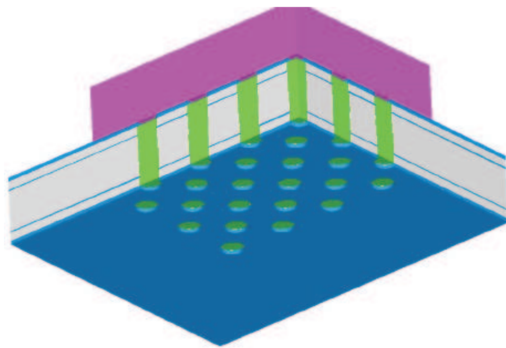

Fig. 10. Diagonal distribution

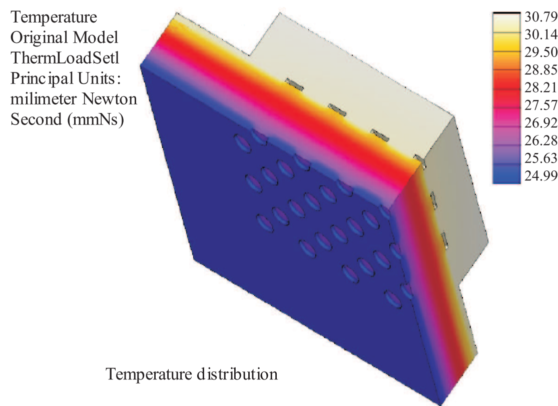

Fig. 11. Temperature values in the case of diagonal distribution

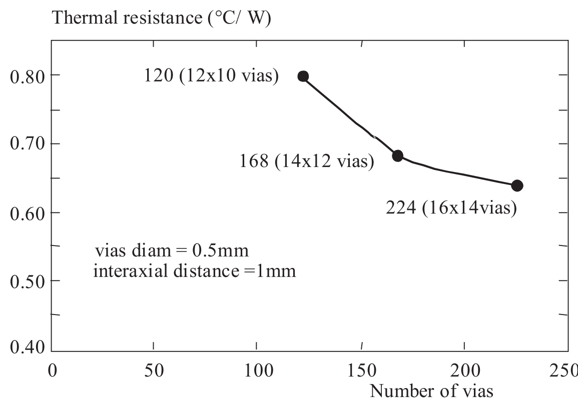

Fig. 12. Thermal resistance vs. number of vias

- inside copper layers have the thickness of 27 μm;
- the external layer thickness is 90 μm; the FR4 has a thickness of 200 μm between the Top (Bottom) layer and the inner layer while between the two inner layers is 966 μm;
- the vias diameter initially considered is 0.5 mm and the minimum distance between two vias axis is two times the diameter (*ie* 1 mm).

The model includes the part of the PCB surrounding the power device with dimensions of 13.68 x 16.28 mm. The TO 220 device has been modeled with a copper plate of 8.89 x 11.49 mm. Thanks to symmetry, a quarter of the complete thermal model has been considered for simulation as shown in Fig. 8.

A thermal power of 1 W (for a quarter) uniformly distributed on the top of the device case, and a uniform temperature of 25°C to the bottom layer represent the load set and the boundary conditions. The obtained temperature distribution is shown in Fig. 9.

As it can be noticed, the maximum temperature is about 29.85°C. The total elapsed time of thermal simulation has been 2760.77 seconds (46 minutes, approximately). The thermal resistance is

$$R_{th} = (29.85 - 25)/(4 * 1) = 1.21(°\mathrm{C/W}).$$

For the same type of PCB with the same dimensions and thicknesses of component materials, a diagonal distribution of vias has been considered. The vias diameter is 0.5 mm and the distance between axes 1 mm. Thanks to symmetry, just one quarter of complete model has been simulated, Fig. 10.

In this case the maximum temperature value is about 30.78°C and the total elapsed time of simulation was 3246 seconds (54.1 minutes). The thermal resistance is

$$R_{th} = (30.78 - 25)/(4 * 1) = 1.445(°\mathrm{C/W}).$$

The thermal simulation conditions were the same like in the case of linear distribution, a thermal power on a quarter of complete model about 1 W and a uniform temperature of the bottom of 25°C. The obtained temperature distribution is shown in Fig. 11.

3.3. Power PCB optimization

With the aim of optimizing the number of vias and their distribution on the PCB, a series of thermal simulations have been done. All the simulations have been performed using the simplified vias model as shown in the first paragraph.

The first configuration studied is a linear distribution of vias with diameter of 0.5 mm and distance between axes 1mm. Thanks to the symmetry the simulation has been performed a quarter of whole thermal model. The total thermal power is $4 \times 1 = 4$ W and the temperature of the bottom layer of the PCB has been fixed to 25°C.

The vias were fully distributed on the PCB surface, so it resulted the number of 16 x 14 = 224 vias. From the thermal simulation the maximum temperature is 27.56°C and the thermal resistance results to be 0.64°C/W.

The same simulation has been performed also with a full diagonal distribution, as shown in Fig. 10. In this case the number of vias is $9 \times 11 + 12 \times 10 = 219$. The maximum temperature is 27.64°C, thus the thermal resistance results to be 0.66°C/W.

As it can be noted from the above simulations, the two types (linear and diagonal) of vias distributions are substantially equivalent. Thus, for the following optimization procedure only the linear distribution will be considered.

As a second optimization step, a model using only one row of vias beyond the case of the power semiconductor

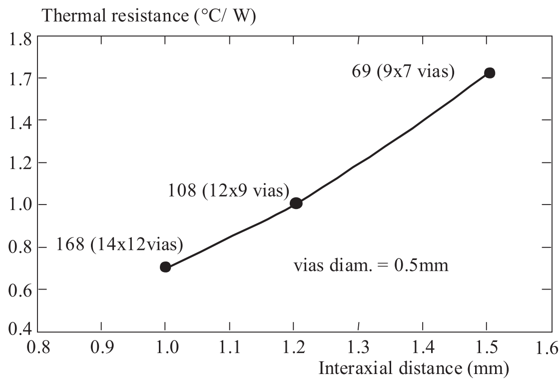

Fig. 13. Thermal resistance vs. distance among vias axes

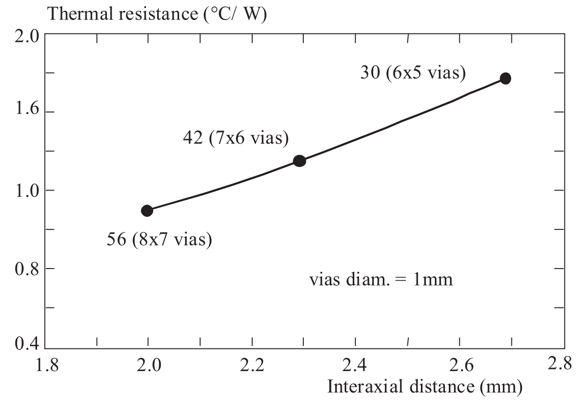

Fig. 14. Thermal resistance vs. distance among vias axes

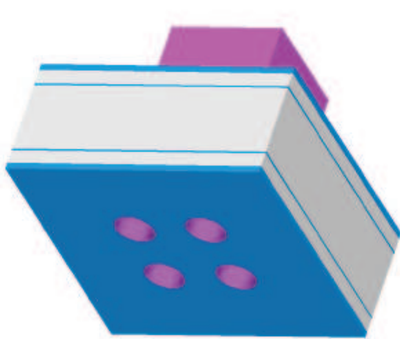

Fig. 15. PCB sample using the full

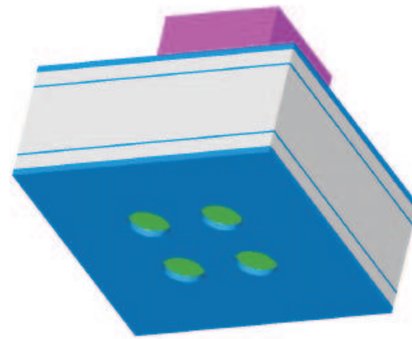

Fig. 16. PCB sample using the simplified vias model

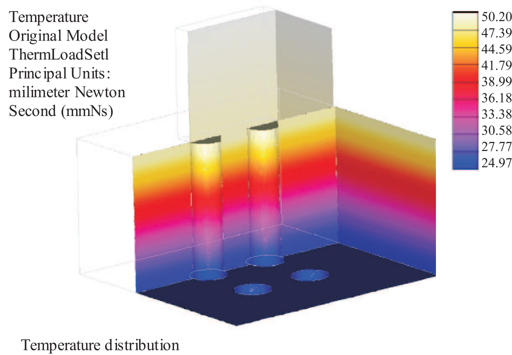

Fig. 17. Simulation results of the PCB sample using the full vias model (4 vias)

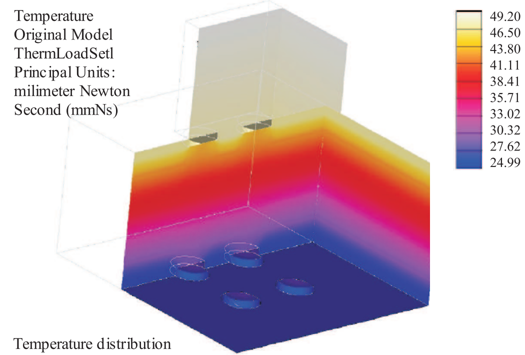

Fig. 18. Simulation results of the PCB sample using the simplified vias model (4 vias)

has been analyzed. In this case, the total number of vias was $14 \times 12 = 168$ with the same diameter and distance among like in the previous case. From the thermal simulation the maximum temperature is 27.75°C with the same total power of 4×1 W. The thermal resistance results in this case 0.6875°C/W.

The third optimization step consists of a linear distribution of vias placed only under the case of power semiconductor. The diameter and the distance among axis were the same like previous cases. The total number of vias is $12 \times 10 = 120$. In this case the maximum temperature is 29.85°C thus, the thermal resistance results in this case 0.8°C/W.

The results obtained from the thermal simulations have been plotted in the chart of Fig. 12. The chart represents the thermal resistance dependence against vias number.

From the below picture it can be observed that the thermal resistance is considerably reduced by adding a row of vias beyond the limit of the device case. This results, for the analyzed geometry, in 168 vias. By adding a second row of vias around the device case, results in a minor change in the thermal resistance value. Because of this, for the next optimization steps, we will consider only the case of one row of vias beyond the device case.

The next parameter on which the optimization has been carried out is the distance between vias. The diameter has been kept constant equal to 0.5 mm.

The first optimization step consisted in increasing the distance to 1.2 mm. This results in a number of vias equal to $12 \times 9 = 108$. The maximum temperature is about 29.01°C and for a total power of 4 W the thermal resistance is 1.0025°C/W. For the next optimization step, the distance has been increased to 1.5 mm. From the thermal simulation the maximum temperature is 31.4°C and the thermal resistance results to be 1.6°C/W.

The results obtained from the above thermal simulations have been plotted in the chart of Fig. 13. The chart represents the thermal resistance dependence against distance between vias axis. From below picture it results that the thermal resistance of the power PCB is approximately proportional to the vias distance.

For the next optimization step the vias diameter has been changed to 1 mm. The distance between vias has been adjusted accordingly to the rule that impose it to be greater than two times the diameter. With this new geometry, the thermal simulations have been repeated with distance among vias axes of respectively 2, 2.3 and 2.7 mm. For these simulations, since the diameter of vias has been changed, a new simplified thermal model of the vias has been developed. For this new vias geometry (using the same approach described in paragraph 3.1.) it has been found that the "ideal" vias filler must have a conductivity of 62.5 N/s°C. Thus, for the distance of 2 mm between vias axes, the maximum temperature is 29.33°C and the thermal resistance for a total power by 4 W is 1.0825°C/W. In the case with 2.3 mm distance among vias axes the thermal resistance is 1.3525°C/W at the total power of 4 W (the maximum temperature is 30.41°C). From thermal simulation in the case of 2.7 mm distance among vias axes, results a maximum temperature of 32.1°C, so the thermal resistance is 1.775°C/W at the same total power of 4 W.

The last three thermal simulations allow to draw a diagram of thermal resistance against the distance between vias axis also for the diameter of 1 mm, Fig. 14.

Also in this case the thermal resistance of the PCB results to be proportional to the distance between the vias. It can be noted that the first value (with 2 mm distance) is very close to the thermal resistance value obtained with 0.5mm vias separated by 1.2 mm distance. The advantage is that in this case the number of vias is 56 instead of 108.

3.4. Validation of the adopted model assumptions

The validation of the vias simplified model has been performed by comparing the results obtained from the simulation of a PCB samples with 4 and 9 vias using the "full model", Fig. 15, with the results obtained from the same PCB sample using the simplified model, Fig. 16. The temperature distributions are shown in Figs. 17 and 18.

For the PCB sample with 4 vias, the simulation using the full vias model results in a maximum temperature of 50.2°C, Fig. 17, that means a temperature rise, ΔT of 25.2°C with respect to the ambient. The simulation of the PCB sample using the simplified model results in a maximum temperature of 49.2°C, Fig. 18, that means a temperature rise, ΔT of 24.2°C with respect to the ambient. For the PCB sample with 9 vias, the simulation using the full vias model results in a maximum temperature of 36.25°C that means a δT of 11.2°C with respect to the ambient. The simulation of the PCB sample using the simplified model results in a maximum temperature of 35.7°C that means a ΔT of 10.7°C with respect to the ambient. The above results in an error of about 4 % on the thermal resistance value which changes only slightly (0.2 %) passing from 4 to 9 vias. This can be regarded as a sort of worst case analysis. In fact, the simulated vias are place right beneath the device case and, thus, are the ones subjected to the highest flux density.

4 CONCLUSIONS

The study of the optimum vias distribution and geometry relatively to the analyzed power PCB application has been performed by means of the following steps:

- setup of a simplified model of the thermal vias;
- setup of the thermal model of the power PCB;
- thermal simulation of the power PCB;
- optimization of the vias distribution and geometry.

For what concerns the last point, the following relevant information have been obtained:

- the number of vias rows has a relevant impact on the thermal resistance up to one row beyond the limit of the device case. Increasing the number of rows further do not give any advantage in thermal of thermal resistance;
- the power PCB thermal resistance is directly proportional to the distance between the vias;
- probably the best trade-off between number of thermal vias and thermal resistance is obtained with 1mm vias separated by 2 mm. This, of course, must be weighted with technological consideration on the manufacturability of this type of solution such as problems with solder leakage, *etc.*

Acknowledgments

The author has a pleasure to acknowledge that described investigations were carried out in the frame of CEEX National Programme, Funding Application for Excellences Research Projects, Code project 5, Contract no. 1489/07.04.2006.

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