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New compensation ferrometer design

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The compensation ferrometer is an instrument for the measurement of open specimen soft magnetic materials parameters at AC magnetization based on the magnetomotive force compensation method. New magnetizing process regulator that controls voltage induced in measuring winding (magnetic flux density waveform) and the voltage induced across Rogowski-Chattock potentiometer (compensation) was developed recently. This paper deals with a new compensation ferrometer design that allows taking the full advantage of the new regulator. New ferrometer based on STEMlab platform improves precision and speed of the measurement.

K e y w o r d s: compensation ferrometer, magnetizing process control, soft magnetic materials

1 Introduction

The compensation ferrometer requires an effective magnetizing control. Two conditions must be fulfilled during measurement. The first condition specifies waveform of the voltage induced in the measuring winding. This voltage is related to the magnetic flux density waveform. The standard requires sinusoidal voltage induced in the measuring winding with form factor $1.11 \pm 1\%$. The second condition is given by the compensation method principle. Voltage induced in the Rogowski-Chattock potentiometer must be zero at any time. New magnetizing process regulator published in [1] based on the compensation ferrometer magnetizing equipment model [2] improves overall magnetizing process control quality. The advantage of the regulator is a control of both conditions as one task. It uses the state feedback that requires outputs calculation on a sample basis. These quick calculations are impossible in the compensation ferrometer KF9a [3] with the old digital part design. The feedback loops are different and analog feedback loops are no longer required therefore analog part of new ferrometer must be redesigned to meet different criteria. New platform selected for the regulator realization and the compensation ferrometer core is the STEMlab 125-14 (originally Red Pitaya v1.1). The STEMlab is a data acquisition platform based on system on the chip with a size of credit card and open-source software. It is equipped with the Xilinx Zynq 7010 SoC (combination of FPGA and dual-core ARM Cortex A9). It has two analog inputs and two analog outputs with 14-bit resolution and 125 MHz sampling frequency. The user interface of new compensation ferrometer is a web page for modern web browsers.

2 New compensation ferrometer

The STEMlab platform is used for regulator design and also for the measurement result calculations. Therefore, the control PC used in previous versions of ferrometers is no longer a part of new ferrometer. New ferrometer is independent on computer operating system and driver support. Conversion to digital domain is done on the STEMlab instead of PC that eliminates the issue with electromagnetic compatibility inside PC. The STEMlab small size allows closer integration with amplifiers with shorter cables. The other advantage is the galvanic insulation of new ferrometer.

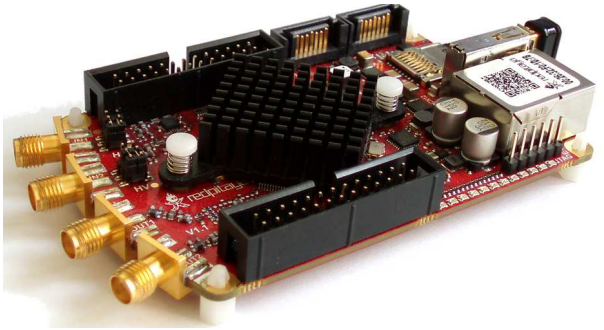

Fig. 1. STEMlab

Magnetizing and compensating voltage amplifiers are DC coupled because AC coupling brings unwanted additional phase shift. Input resistance is 50 Ω according to the STEMlab outputs specifications. The measuring, magnetizing and compensating amplifiers have programmable voltage gain in order to use full voltage range ± 1 V of ADCs and DACs. The amplifiers can communicate with the STEMlab via I^2C or SPI. Amplifiers and converters offsets can also be digitally suppressed by regulator calibration coefficients. DC feedback in regulator

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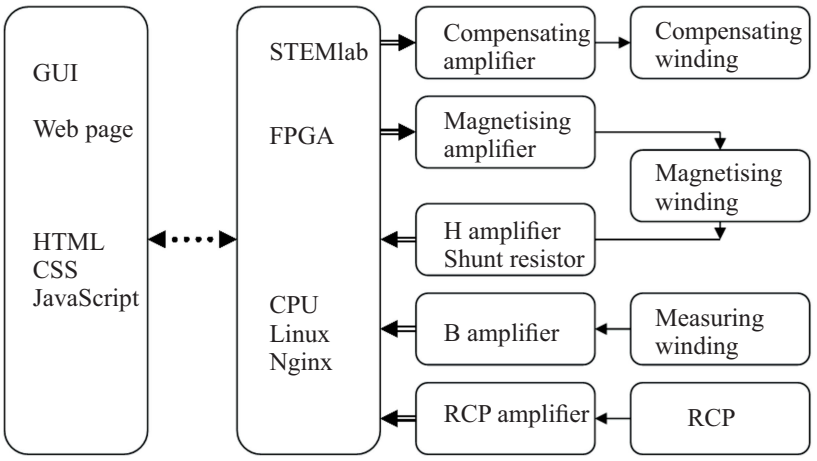

Fig. 2. Compensation ferrometer block diagram

can adjust offsets for the external magnetic field compensation. Symmetry of measured hysteresis loop can be the indicator. Fine tuning of offsets by digital part requires additional low-speed DACs and summing magnetizing and compensating amplifiers because the gain for offset tuning should be smaller than gain for exciting voltages. The maximum magnetizing frequency is limited by the bandwidth of the exciting amplifier. The bandwidth 100 kHz of the amplifiers Apex MP38 used in KF9a limit magnetizing frequency maximum to 10 kHz.

STEMlab has two inputs. The first input is used for the magnetizing current measurement, the second one measures the voltage induced in the measuring winding. The third input is necessary for measurement of the voltage induced in the Rogowski-Chattock potentiometer. The third ADC is connected to the STEMlab extension connector. All measuring amplifiers are low noise differential amplifiers.

The ferrometer user interface is based on a web page hosted by Nginx web server running on the STEMlab. Thus the ferrometer can be used with any device with a modern web browser. STEMlab has 1 Gb/s Ethernet port that with media converter provides an optic link for data transfer. The option for short-distance galvanically insulated connection is Wi-Fi provided by the USB 2.0 Wi-Fi adapter.

3 Regulator

The magnetizing process regulator computes magnetizing and compensating voltage samples based on actual magnetizing current samples and measured hysteresis loop according to (1), (2), (3). n is an index in the table of functions f_1 and f_2 , w_{RCP} is the reference waveform dependent on the voltage induced in the RCP reference, $u_{1\mathrm{rp}}$ is binary representation of the magnetizing current, $u_{1\mathrm{bin}}$ is representation of the magnetizing voltage, w_2 is the magnetizing voltage reference waveform, f_1 and f_2 are functions dependent on the measured hysteresis loop, u_{cbin} is representation of the compensating voltage, and ξ are constants based on magnetizing equipment properties.

$$n = w_{\mathrm{RCP}} + \xi_8 u_{1\mathrm{rp}} \tag{1}$$

$$u_{1\mathrm{bin}} = (w_2 + f_1[n]) f_2[n] + \xi_1 u_{1\mathrm{rp}} + \xi_2 \tag{2}$$

$$u_{\mathrm{cbin}} = \xi_5 f_1[n] + \xi_6 w_{\mathrm{RCP}} + \xi_3 u_{1\mathrm{bin}} + \xi_4 u_{1\mathrm{rp}} + \xi_7 \tag{3}$$

These equations are implemented in FPGA using 32-bit floating-point arithmetic. The input representation of the magnetizing current $u_{1\mathrm{rp}}$ is taken from the 14-bit ADC converter connected directly to FPGA. Sampling frequency is 125 MHz. Both outputs are connected to the 14-bit DAC converters also with sampling frequency 125 MHz. Calculation algorithm takes 75 cycles of 125 MHz clock. The output sampling frequency is 1.66 MHz only because FPGA is not used at the maximum clock frequency and the feedback algorithm uses slower floating-point arithmetic instead of faster fixed-point arithmetic.

The reference waveforms are generated by two channels synchronous arbitrary signal generator with classic structure implemented in FPGA. It works natively with frequency 125 MHz. Each waveform has 16384 32-bit floating point samples. The maximum frequency error for full buffer length is 58.2 mHz. This error can be decreased using a shorter buffer or increasing generator index precision (use more bits) if necessary.

The regulator needs to know if the actually computed point belongs to ascending or descending part of the measured hysteresis loop in order to select correct values of functions f_1 and f_2 . The decision about increasing or decreasing magnetic field strength is based on the magnetizing current. Magnetizing current is selected because the reference wRCP is small and it has no influence on the decision. The decision is made by the logic module in FPGA. It firstly filters $u_{1\mathrm{rp}}$ by low pass filter (4) to suppress noise. N used by the filter is a power of two. The filter is implemented in fixed-point arithmetic. The group

delay of the filter should be constant for the frequencies relevant to the magnetizing current

$$u_{1\mathrm{rpfilt}}[k] = \frac{u_{rm1rp}[k] + (N-1)u_{1\mathrm{rpfilt}}[k-1]}{N} \quad (4)$$

The logic module is counting consecutive cycles where the maximum (minimum) value of the filtered magnetizing current $u_{1\mathrm{rpfilt}}$ is unchanged. If the counted value overcomes defined threshold the minimum (maximum) value is reset and the output is set to $u_{1\mathrm{rpfilt}}$ is decreasing ($u_{1\mathrm{rpfilt}}$ is increasing) value. To prevent the false output switching, there must elapse more time then the specific dead time between two output changes. The minimum (maximum) value of the $u_{1\mathrm{rpfilt}}$ maximum (minimum) must be above (under) some limit value to prevent the local extreme false evaluation and the output change. The output of the logic module adding offset to the index n that lead to selecting correct part of the functions f_1 and f_2 tables. Delay that decision takes is an important property of the logic module. It is 142 μs for the robust setting of the logic module at measurement frequency 50 Hz, but the logic module interval is only 6 cycles of 125 MHz clock (48 ns).

4 Results processing

STEMlab is also used for the measurement. Data acquisition module in FPGA that is independent on the regulator is used for acquiring measured inputs samples. This module decimates data to reduce the amount of data transferred to CPU accessible memory because STEMlab has 512 MB RAM. The module also filters data for the inputs characteristic equalization. The data are processed in CPU.

STEMlabs inputs and outputs have common 125 MHz clock signal, but the data acquisition module measurement start time and regulator start time are independent. Regulator works continuously, while data acquisition module works only at a command from ferrometer software. The synchronization is made by a trigger that is sent from the regulators signal generator module to the data acquisition module at the start of each magnetizing signal period. If the data acquisition module acquires data, then the trigger is ignored.

STEMlab uses operating system Linux (Ubuntu) that run on CPU. The FPGA is operating via user-space drivers (UIO interface). Ferrometer software runs as Nginx module. It computes results from the measured data and also one period of the reference waveforms and tables of the functions f_1 and f_2 for the regulator. Results as hysteresis loop, specific loss power, *etc*, and processed waveforms are periodically sent to the web page GUI using WebSocket protocol. FPGA is programmed in Verilog, software in C++ and web page in JavaScript and HTML+CSS.

Ferometer software starts at Nginx request when a user loads the web page interface. FPGA bit file for the compensation ferrometer is uploaded to FPGA. Software uses two threads. The first thread is dedicated to the communication with Nginx and user interface. Communication with Nginx is based on several functions that are periodically called. The application has two type of messages: parameters and signals. The parameters contain a single value, and they are used for control of measurement and a single value results transfer. The signals contain arrays, and they are used to transfer measured waveforms and hysteresis loop. Both messages type is saved in JSON (JavaScript Object Notation) format and optionally compress by gzip library for transmitting. JSON format is human readable, and it is easily convertible to

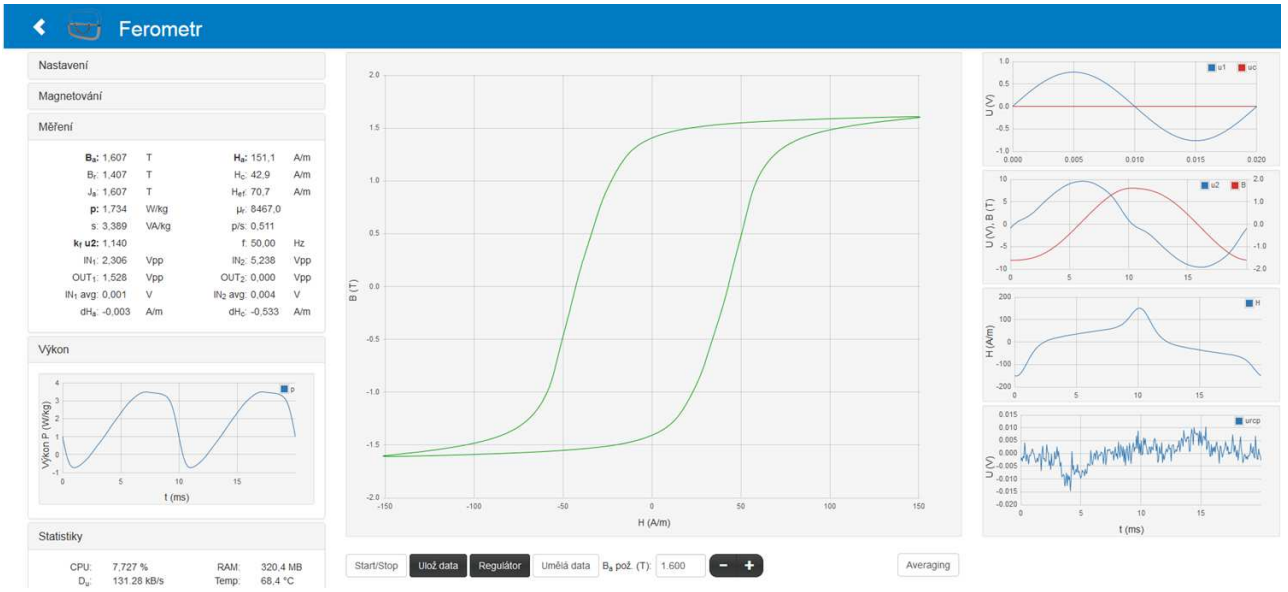

Fig. 3. Ferrometer GUI

JavaScript object. On web page side the JavaScript take care of WebSocket communication, decompression of data and creating an object from JSON messages. The web page is periodically updated with actually available data and control commands. The flot library (JavaScript) is used for graphs plotting. The results of measurement are not processed in web browser although it is possible to make some calculation in JavaScript.

The second thread is used for the measurement control and result processing. It repeats following steps. It checks control parameters. If the parameters are changed then new values are set. The data acquisition module is started. It acquires samples that cover 30 periods of the magnetizing voltage. Then the measurement results are computed. They are saved to the internal structure of thread. The next step is the computation of function tables for the regulator and reference waveforms if they are required. Computed values for the regulator are transferred to the FPGA accessible memory and results of the measurement are transferred to the first thread for the transfer to the user interface. The necessary thread synchronization is based on the mutex. This processing scheme does not process every period. It does not measure continuously, but it is possible to measure continuously for the low magnetizing frequency at least.

5 Conclusion

New compensation ferrometer improves precision and speed of the measurement. The reason is the new magnetizing process regulator. Presented design is standalone without dependence on the control PC and galvanically insulated. The processing on the SoC (FPGA+CPU) is flexible and allows update in future, for example, faster regulator processing in fixed-point arithmetic, use of information about periodicity in the logic module or continuous measurement.

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