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PAPERS

Low-noise and low power CMOS photoreceptor using split-length MOSFET

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This paper presents the design of a low-power and low-noise CMOS photo-transduction circuit. We propose to use the new technique of composite transistors for noise reduction of photoreceptor in the subthreshold by exploiting the small size effects of CMOS transistors. Several power and noise optimizations, design requirements, and performance limitations relating to the CMOS photoreceptor are presented. This new structure with composite transistors ensures low noise and low power consumption. The CMOS photoreceptor, implemented in a 130 nm standard CMOS technology with a 1.2 V supply voltage, achieves a noise floor of $2\,\mu V/\sqrt{Hz}$ within the frequency range from 1 Hz to 10 kHz. The current consumption of the CMOS photoreceptor is 541 nA. This paper shows the need for the design of phototransduction circuit at low voltage, low noise and how these constraints are reflected in the design of CMOS vision sensor.

K e y w o r d s: photo-receptor, image sensor, low-noise, low-power, cmos circuit

1 Introduction

Nowadays, applications of vision sensors require incessantly increasing spatial resolution (number of pixels) and temporal resolution (number of frames per second) and leading to a large volume of output data and increasing demands on the bandwidth of transmission, storage and power processing [1]. In parallel, cost and power consumption have become increasingly restrictive especially for mobile applications. Another crucial performance criterion for a vision sensor is its dynamic range (DR). This quantity is usually defined as the ratio between the largest output signal and the noise level in the dark. It is typically limited by the ability of the pixel to integrate photogenerated charges and the time of this integration. The CMOS imaging market evolves very quickly in the field of semiconductor industry. This is mainly due to the increasing adoption of cameras in mobile devices and the rapid development of consumer digital cameras. The major progress which led to the rapid development of CMOS imagers is the evolution of CMOS technology in terms of miniaturization and maturation. In this case, the use of CMOS devices is considered as a great advantage because it provides the potential for implementing pre-processing functions and correcting defects.

Most of the work on complex CMOS systems deals with the integration of sensors providing a processing unit at chip level (system-on-chip approach) or at column level by integrating an array of processing elements dedicated to one or more columns [2]. Indeed, pixel-level processing is generally dismissed because pixel sizes are often too large to be of practical use. However, as CMOS image sensors scale to 0.18 m processes and under, integrating a processing element at each pixel or group of neighboring pixels becomes feasible. More significantly, employing a processing element per pixel offers the opportunity to achieve massively parallel computations and thus the ability to exploit the high-speed imaging capability of CMOS image sensors [3]. This also benefits the implementation of new complex applications at standard rates and improves the performance of existing video applications such as motion vector estimation [4], multiple captures with dynamic range [5], motion capture [6], and pattern recognition [7]. From an industrial point of view, the main design constraint is obviously the pixel pitch (*ie* the pixel surface) to be as small as possible to obtain a large matrix with a reasonable silicon surface. Secondly, we want to have a good fill factor (*ie* the ratio between the photosensitive surface and the total pixel surface) and finally, we want to design devices with the lowest noise and the lowest power consumption.

In this letter, we present a new structure of a CMOS photoreceptor, suited to low power consumption, low noise and high linearity, while simultaneously ensuring a low pixel pitch and a high fill-factor. This new structure is based on the technique of composite transistors.

2 Split-length MOS transistor analysis

Despite a regular MOSFET and a split-length MOS transistor have the same geometrical structure; however,

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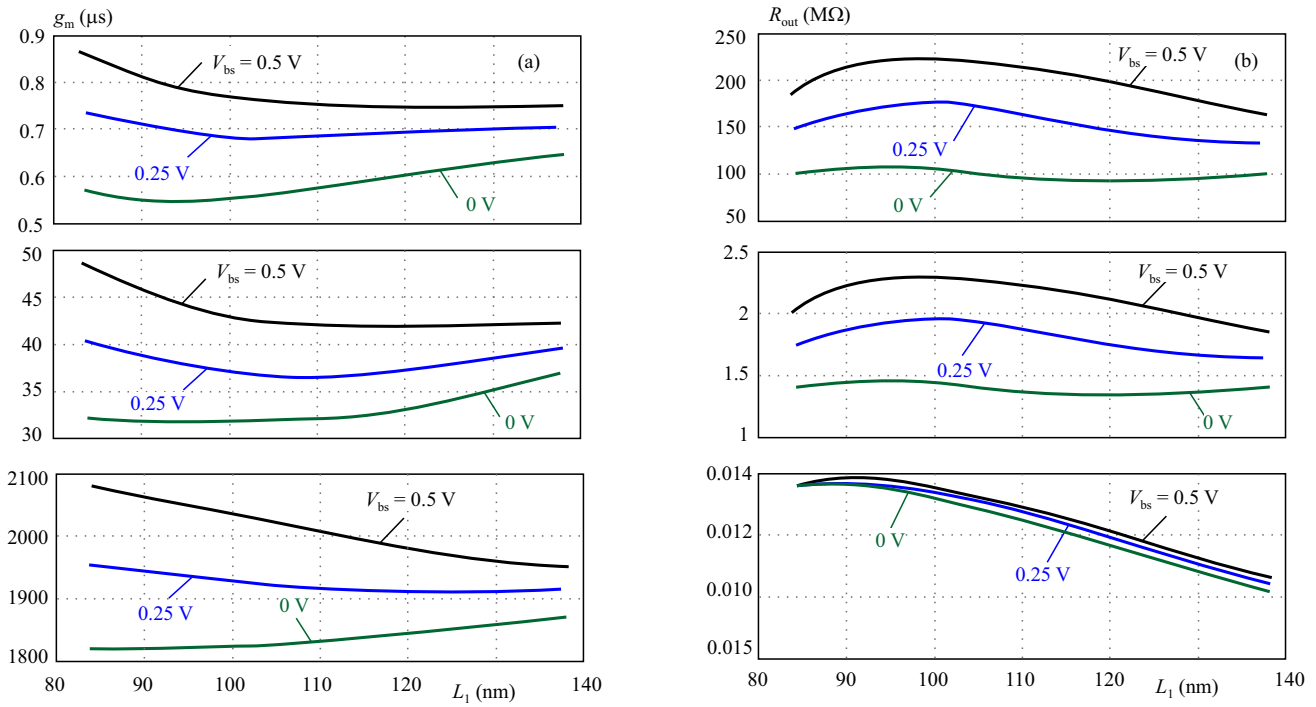

Fig. 1. Simulation results of the split-length MOS transistor: (a) – transconductance of SLT ($W = 10$ μm and $L = 0.13$ μm), (b) – output resistance of SLT

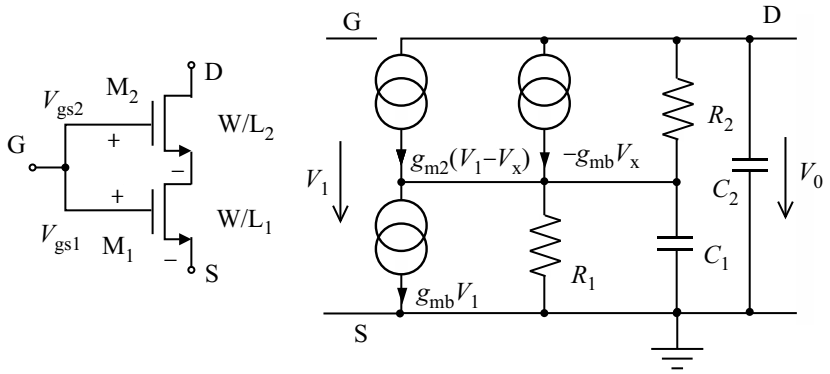

Fig. 2. Split-length MOS transistor with the small-signal equivalent model

the second transistor has a better transconductance and output resistance than the first one. If the regular metal-oxide silicon field-effect transistor (MOSFET) is used to enhance the gain, then it requires a long channel. Else, if the same regular MOSFET is used to increase the speed, then it requires a short channel. The split-length MOS transistor has a major asset compared to the regular MOSFET. With the same channel length, the split-length MOS transistor will increase the gain without affecting the speed.

The small signal model of a split-length MOS transistor is shown in Fig. 2 [8, 9]. Transistors M1 and M2 are tied together. Moreover, they have the same width W and their lengths are L_1 and L_2 respectively. The common-gate voltage V_g of split-length MOS transistor specify the operating regions of transistors M1 and M2. To identify the operating region of a transistor, we compare its V_g with its threshold voltage $V_{\rm th}$. In this case, if V_g is greater than $V_{\rm th}$ of both M1 and M2, then M1 operates in linear region and M2 operates in saturation region. In addition, $V_{\rm th}$ of drain transistor M2 decreases because of the bulk bias. Therefore, the drain-source voltage $V_{\rm ds}$ of source transistor M1 increase. As a result, the operating region of M1 moves from linear inversion region to the edge of saturation or moderate inversion region.

The output resistance of the split-length MOS transistor with bulk bias is

$$R_{\rm out} = r_1 + r_2 + (g_{m2} + g_{mb})r_1 r_2 = (g_{m2} + g_{mb})r_1 r_2 \quad (1)$$

and describes its output resistance with positive feedback

$$R_{\rm outp} = \frac{r_1 + r_2 + (g_{m2} + g_{mb})r_1 r_2}{1 - g_{mb} r_2}. \quad (2)$$

If $g_{\mathrm{mbr2}} > 1$, then R_{outp} is negative. In addition, the split-length MOS transistor input transconductance is

$$g_m = \frac{g_{m1}r_1 + g_{m2}r_2 + g_{m1}(g_{m2} + g_{mb})r_1r_2}{r_1 + r_2 + (g_{m2} + g_{mb})r_1r_2}\,. \quad (3)$$

First, simulations of parameter g_{m} of n-channel split-length MOS transistor are carried out for different gate and bulk voltages of M2. Then, simulations of its parameter $R_$out are also performed. Results are shown in Fig. 1(a) and Fig. 1(b). Looking at the characteristics of Fig. 1(a), we can conclude that a higher value of transconductance g_{m} can be achieved if the channel length L_1 has a short value. Moreover, the total effective transconductance g_{m} decrease if the length L_1 increase. Similarly, for the p -channel split-length MOS transistor, its small-signal parameters are extracted to design the proposed two-stage OTA.

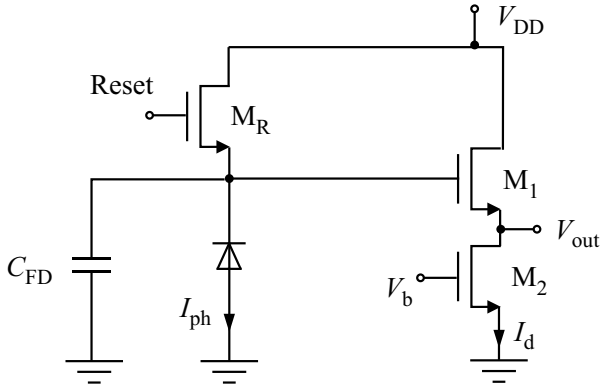

Fig. 3. Circuit of the classical CMOS photoreceptor

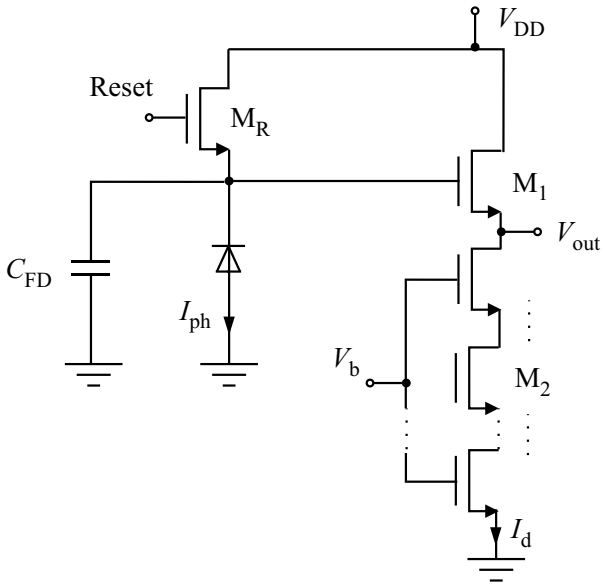

Fig. 4. Circuit of the new CMOS photoreceptor

3 New CMOS photoreceptor circuit

We have different alternatives to design a CMOS photoreceptor circuit. The most popular architecture is the source follower readout circuit [10, 11]. As shown in Fig. 3, a two-transistor active pixel sensor is connected to an ideal current source and forms a source follower readout circuit. Transistors M1 and M2 act as a source follower. It operates in saturation zone because $V_{\mathrm{ds}} > (V_{\mathrm{gs}} - V_{\mathrm{th}})$.

If two transistors operate in strong inversion and are in saturation, the expression for the current Id flowing through transistor M2 is

$$I_d = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W_2}{L_2}(V_{\mathrm{gs2}} - V_{\mathrm{th}})^2(1 + \lambda V_{\mathrm{ds2}}) \quad (4)$$

where V_{ds2} the drain-source voltage of M2, V_{gs2} the gate-source voltage of M2, λ the channel length modulation constant, W_2 the channel width of M2, L_2 the channel length of M2, C_{ox} the gate oxide capacitance per unit area, V_{th} the threshold voltage and μ represents the effective mobility of M2. The channel length modulation constant λ can be written as

$$\lambda \approx \frac{1}{L_2}\,. \quad (5)$$

The transconductance g_{m} of transistor M2 can be written as

$$g_m = \sqrt{\frac{2\mu C_{\mathrm{ox}}(W_2/L_2)I_d}{1 + \lambda V_{\mathrm{ds2}}}}\,. \quad (6)$$

Equation (4) shows that the current transfer function is dependent on the bias voltages of input and output nodes of the transistor M2 $(\lambda.V_{\mathrm{ds2}})$. Hence, λ introduces a non-linearity as a function of the output voltage V_{out} [12]. As process technology scales, however, the area occupied by the pixel transistors decreases, providing more freedom to increase fill factor while maintaining a small pixel size. For this reason, we use transistors with a very small W/L ratio to determine the optimal pixel fill factor. This source follower architecture introduces a non-linearity and errors due to the channel length modulation λ. With low-voltage submicron technologies and with a channel length L close to the minimum value, we often seek to improve the current source output characteristics because the parameter λ have very high values in these technologies. The total current consumption of this classical source follower is I_d. We often seek also to reduce its noise and current consumption.

To improve the architecture of the CMOS photoreceptor while improving a low current consumption and removing the λ effects, we propose to use a new technique of composite transistors. The structure of the new CMOS photoreceptor circuit is presented by Fig. 4. It is composed of a reset switch Mreset and a source follower realized by transistor M1 and N transistors M2. The output will be between the transistors M1 and the first transistor M2.

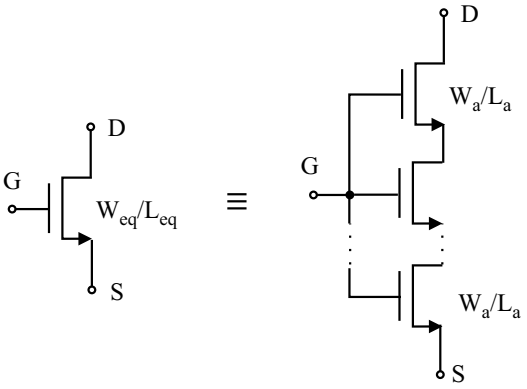

Fig. 5. Composite transistor with equivalent channel length $L_{\rm eq} = NL_a$

Figure 5 shows the concept of the composite transistor technique. We have N transistors NMOS in series with the same sizes $W_{\rm a}/L_{\rm a}$. These N transistors NMOS form our composite structure. In this case, the N transistors are equivalent to a single transistor with an equivalent channel length $L_{\rm eq} = N\,L_{\rm a}$ and an equivalent width $W_{\rm eq} = W_{\rm a}$. The new CMOS photoreceptor circuit is based on this technique. Our idea is to use this technique to reduce noise and power consumption and to improve the linearity with minimizing λ.

Starting from the polarization of the composite transistor, the expression for the current I'_d flowing through transistors is

$$I'_d = \frac{1}{2}\mu C_{\rm ox}\frac{W_2}{NL_2}(V_{\rm gs2} - V_{\rm th})^2(1 + \lambda V_{\rm ds2}) = \frac{I_d}{N}\,. \quad (7)$$

The equivalent channel length modulation constant λ' of the composite transistor can be written as

$$\lambda' \approx \frac{1}{NL_2} = \frac{\lambda}{N}\,. \quad (8)$$

The equivalent transconductance $g'_{\rm m}$ of the composite transistor can be written as

$$g'_{\rm m} = \sqrt{\frac{2\mu C_{\rm ox}(W_2/NL_2)I_d}{1 + \lambda V_{\rm ds}}} < g_{\rm m}\,. \quad (9)$$

According to (7), if the number N of transistors placed in series increase, the drain-source current I'_d becomes I_d/N. The total current consumption of the new CMOS photoreceptor decreases by a factor of $1/N$. Furthermore, if N increases, the channel length modulation constant λ' becomes λ/N. The non-linearity due to λ effects decreases by a factor of $1/N$. This new structure ensures suppression of errors and non-linearity due to the λ effects. This new architecture improves low current consumption and high linearity of a CMOS photoreceptor structure due to the use of N transistors in series.

The noise sources of the CMOS photoreceptor originate from flicker noise and thermal noise components. The flicker noise component is usually larger than the thermal noise component for low frequency for typical bias conditions and device geometries. The total noise current of a MOSFET from the Razavi noise model is given as

$$\overline{v_{n,m}^2} = \frac{8KT}{3}\Big(\frac{1}{g_{\rm m1}} + \frac{g_{\rm m2}}{g_{\rm m1}^2}\Big) + \frac{1}{C_{\rm ox}f}\Big(\frac{K_n}{W_1L_1} + \frac{K_n}{W_2L_2}\frac{g_{\rm m2}^2}{g_{\rm m1}^2}\Big) \quad (10)$$

where, K denotes the Boltzmann constant, K_n denotes the flicker noise coefficient of NMOS transistors, $C_{\rm ox}$ the gate oxide capacitance per unit area, f the frequency, W the channel width, L the channel length and T the temperature in Kelvin.

According to (10), if we want to minimize the noise, one solution is to decrease the transconductance $g_{\rm m2}$ of the transistor M2. To decrease the transconductance $g_{\rm m2}$ of the transistor M2, we must increase the channel length L of the transistor M2. According to (9), if the number N of transistors placed in series increase, the transconductance $g'_{\rm m}$ of the equivalent transistor M2 decrease and becomes lower than $g_{\rm m}$. Our new architecture decreases the transconductance of the equivalent transistor M2 using the composite method, therefore, decreasing the total noise of CMOS photoreceptor. This new architecture is based on the design of N transistors of source follower in series thereby decreasing its transconductance and minimizing its noise.

The new CMOS photoreceptor circuit is simulated using transistor model parameters of the CMOS 130 nm technology at a 1.2 V power supply voltage. The active circuit is composed by the photodiode and the readout circuit. The test chip occupies 30mm × 30mm, high-resistive polysilicon resistors and metal-insulator-metal (MIM) capacitors has been adopted for passive devices due to their high linearity. A series of simulation experiments were conducted to measure the performances of the new architecture of CMOS photoreceptor. To validate our new circuit of CMOS photoreceptor, we have performed several simulations for $N = 1$, $N = 2$ and $N = 3$. We use Cadence® Spectre® and with all transistors having small sizes $W/L = 150/130\,({\rm nm/nm})$.

At the same simulation condition, the total current consumption of CMOS photoreceptor with $N = 3$ is three times lower than that of a CMOS photoreceptor with $N = 1$ and the total current consumption of CMOS photoreceptor with $N = 2$ is two times lower than that of a CMOS photoreceptor with $N = 1$. Total current consumption of CMOS photoreceptor with $N = 3$ is 541 nA only and for a CMOS photoreceptor with $N = 2$ is 826 nA only compared to a CMOS photoreceptor with $N = 1$ which is 1.74μA. The simulated output noise for CMOS photoreceptor and CMOS photoreceptor with N transistors $V_{n,\rm out}$ in the 1 Hz–10 kHz bandwidth are plotted in Fig. 6. For small $I_{\rm ph}$, $V_{n,\rm out}$ for $N = 1$ is equal to $10\,\mu$V. $V_{n,\rm out}$ for $N = 2$ and 3 is equal to $7\,\mu$V and $2\,\mu$V respectively. As $I_{\rm ph}$ increase, shot noise contribution decreases, and transistor $1/f$ noise becomes prominent. $V_{n,\rm out}$ for $N = 1$ saturates to $0.1\,\mu$V at

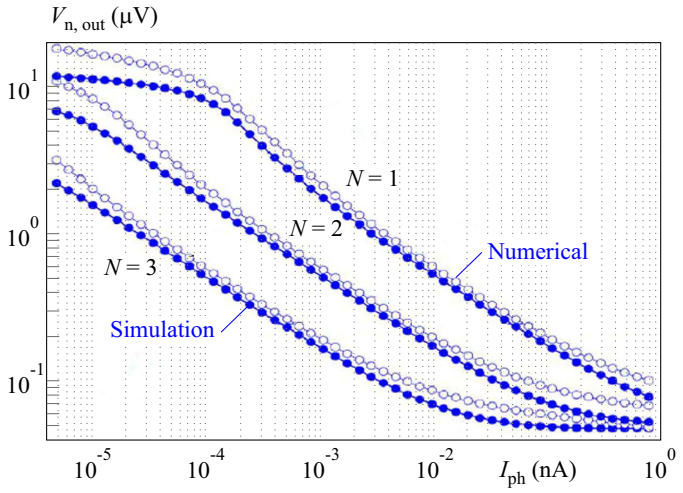

Fig. 6. Noise comparison of CMOS photoreceptor with $N = 1, 2, 3$

Table 1. Performance summary of the photoreceptor circuit, CMOS 130 nm

N	1	2	3
Supply voltage (V)	1.2	1.2	1.2
Current consump. (μA)	1.74	0.826	0.541
Noise (μV) @ 100 Hz	10	7	2
Noise (μV) @ 1 kHz	0.1	0.06	0.05

Table 2. Performance summary of the composite transistor, CMOS 130 nm

	W1/L1	(W2/L2)	(W3/L3)
Supply voltage (V)	1.2	1.2	1.2
Current consump. (μA)	2.73	0.948	0.541
Noise (μV) @ 100 Hz	10.5	6.6	2
Noise (μV) @ 1 kHz	0.9	0.12	0.05

$I_{\rm ph} = 1$ nA. $V_{n,\rm out}$ for $N = 2$ and 3 continues to decrease and saturates to 0.06 μV and 0.05 μV respectively at about $I_{\rm ph} = 1$ nA. CMOS photoreceptor with N transistors noise is lower compared to a classical CMOS photoreceptor noise. At the same simulation condition, the total current consumption of the new CMOS photoreceptor is $1/N$ times lower than that of a conventional photoreceptor. If N increases, the total noise of the new CMOS photoreceptor decreases compared to a conventional photoreceptor noise. if N increases, the channel length modulation constant λ' becomes λ/N. This new structure ensures suppression of errors and non-linearity due to the λ effects. The results of circuit simulation in a standard 130 nm CMOS process for the new CMOS photoreceptor and the conventional photoreceptor are summarized in the following Tab. 1. The numerical simulation output noise of CMOS photoreceptor for $N = 1$, 2 and 3 with Matlab@ are also plotted in Fig. 6. Numerical simulation with Matlab@ and transistors simulation with Cadence@ Spectre@ are approximately the same. In a direct comparison of the CMOS photoreceptor, if N increases, the total noise decreases. CMOS photoreceptor with N transistors shows a reduction in quiescent noise and current consumption at minimum size W/L.

A series of simulation experiments were also conducted to measure the performances of the technique of composite transistor. To validate our new circuit of CMOS photoreceptor, we have performed several simulations. The first one is with a single transistor with a size of $W_1/L_1 = 450/130$ (nm/nm). The second one is with two transistors with a size of $W_2/L_2 = (W_1/L_1)/2$ for each transistor. In this case, we split the transistor W_1/L_1 into two transistors. The third one is with three transistors with a size of $W_3/L_3 = (W_1/L_1)/3$ for each transistor. In this case, we split the transistor W_1/L_1 into three transistors. The results of circuit simulation in a standard 130 nm CMOS process are summarized in the following Tab. 2. The simulation experiments show the improvement of the noise and current consumption by exploiting the technique of composite transistor.

4 Conclusion

We have presented a new low noise and low power architecture of a CMOS photoreceptor circuit. The new idea is to use the technique of a composite transistor for noise and power consumption reduction of photoreceptor. This new structure ensures suppression of errors and nonlinearity due to the λ effects. This new structure ensures low noise, low power consumption and high linearity because of composite transistor. It ensures also high fill factor due to the use of small size transistors. This solution allows us to have an original CMOS photoreceptor readout circuit with low noise and low power consumption. Moreover, the low noise and high fill factor are very useful when the power consumption budget is limited. Our new CMOS photoreceptor provides a power consumption

and noise significantly lower than that of a conventional photoreceptor circuit.

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