

# Low-power latch comparator with accurate hysteresis control

Leïla Khanfir<sup>1</sup>, Jaouhar Mouïne<sup>2</sup>

Recent research has focused on finding ways to control hysteresis of dynamic comparators. The current proposed techniques are based on either geometrical dimension adjustment or digital control. The first case does not allow for post fabrication control, while the second has limited accuracy. This paper presents a new dynamic comparator design with external hysteresis adjustment using an analog voltage. This is achieved by proposing an architecture including control devices with a specific sizing. This is performed with no significant increase of the design complexity, keeping the power consumption as low as possible. The design is analyzed, showing that the proposed solution allows accurate hysteresis adjustment without affecting the inherent circuit properties. The dynamic comparator is also implemented using a 180 nm commercially available CMOS technology. The results show that a variation of 550 mV of the control voltage allows an accurate hysteresis adjustment ranging from 0 to 40 mV, according to the input conditions. Moreover, the simplicity of the circuit in conjunction with the use of dynamic technology have allowed the best performances to be achieved compared to the current state of the art, in terms of energy with an FoM equal to 116 fJ/decision and silicon area of 180  $\mu\text{m}^2$ .

**Keywords:** dynamic comparator, hysteresis analysis, hysteresis control, low power, Schmitt trigger

## 1 Introduction

Today, the ever-increasing demand for full performances, including operation speed, power consumption, silicon area and accuracy, is making the circuit design in modern electronic systems tedious and challenging. If speed, power and area can be optimized by using dynamic circuits, accuracy can be more easily ensured using static ones. Good accuracy can also be achieved using dynamic circuits, but this generally requires complex calibrating schemes [1-4].

Dynamic operation is mainly based on the charge and discharge of internal capacitors [5]. As a result, speed optimization can be achieved by simply minimizing the devices' dimensions which also optimizes the power consumption and the silicon area. However, the circuit analysis must consider parasitics which increases the complexity of analytical developments [6]. The latter are crucial to achieve optimal performance, especially in dynamic circuits. Therefore, thorough analyzes have been undertaken on the dynamic comparator in order to meet the stringent requirements of full circuit performances [69].

Recent works allowed defining hysteresis in dynamic comparators [6]. This circuit property is a prime characteristic of Schmitt triggers (STs) and is usually set to appropriate values to achieve a desired function. STs are largely used in threshold-based applications such as biomedical equipment [10], electromagnetic energy transducers for energy harvesting [11], audio amplifiers [12], square and triangular wave generators [13] and Li-ion battery characterization [14].

Current techniques for hysteresis control in static and dynamic comparators use Complementary Metal Oxide Semiconductor (CMOS) [10, 15-17], Floating-Gate MOS (FGMOS) [18], and Bipolar CMOS [19] silicon technologies. All these have achieved comparable hysteresis control ranges. However, the best energy efficiency was obtained when using dynamic CMOS circuits [16, 17]. Although good accuracy was achieved in [16], the presented technique is geometry-dependent, and no external adjustment could be made. The work in [17] presents another solution that relies on the use of an advanced comparator structure and additional circuitry for clock delay control, which considerably increases the design complexity. Moreover, it is based on digital control which limits the adjustment accuracy.

This work presents a new dynamic comparator with accurate hysteresis adjustment. It achieves a very good accuracy, while controlling hysteresis with an external analog voltage. The hysteresis is analyzed and determined showing that the proposed design allows for accurate control without trading any circuit performance. On the other hand, the resulting circuit remains simple, effective, accurate and presents high performances compared to current works [15-20].

After introducing the hysteresis in dynamic comparators, we present the new design of the dynamic comparator with accurate hysteresis control. The theoretical analysis of its related hysteresis is also exposed. The assumptions are then confirmed by a computer-based analysis. Finally, we describe the proposed circuit implementation,

<sup>1</sup>Laboratory of Analysis, Design and Control of Systems, University of Tunis El Manar, National Engineering School of Tunis, Tunis, 1002, Tunisia, <sup>2</sup>Department of Electrical Engineering, College of Engineering, Prince Sattam Bin Abdulaziz University, Al Kharj, 11942, Saudi Arabia, j.mouine@psau.edu.sa

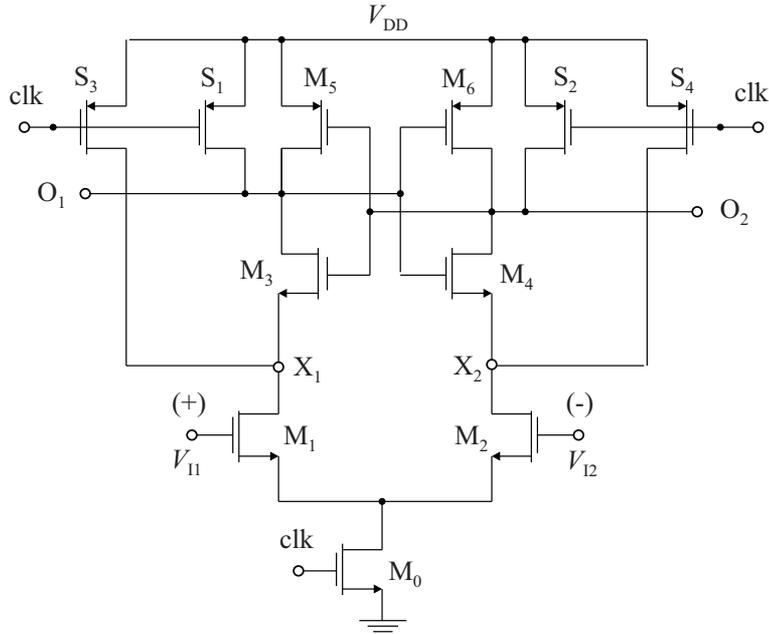


Fig. 1. Basic strong-arm sense amplifier

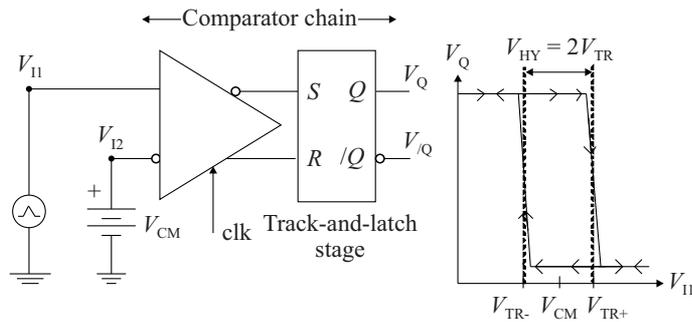


Fig. 2. Hysteresis window in latch comparators

simulation, and characterization, as well as the comparison of its performances to the state-of-the-art results.

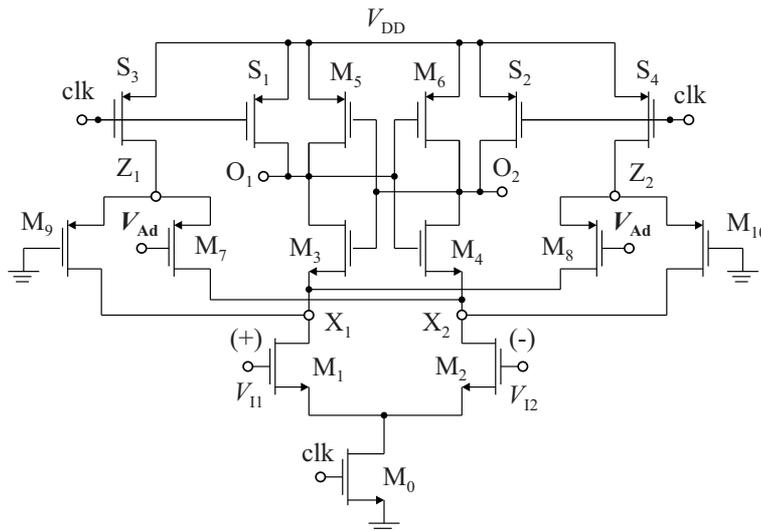
## 2 Hysteresis in latch comparators

Latch comparator, also known as dynamic comparator, is a key building bloc in many electronic systems such as Analog to Digital Converters (ADC) [21], Static Random Access Memory (SRAM) bit line detectors [7], battery-based sensing systems [4], and high-performance electronic devices in general. Figure 1 presents the strong-arm sense amplifier, which is one of the most used latch comparator structures in high performance microelectronic design. This circuit is formed by a latch  $M_{3-6}$ , which is controlled by an input pair transistor  $M_{1,2}$  and biased by a tail transistor  $M_0$ . Four PMOS transistors  $S_{1-4}$  operate as switches to discharge the latch internal capacitors during the reset phase prior to each decision process. Thus, the latch comparator operates over two phases reset and decision.

The reset phase begins when the clock  $clk$  goes low. The tail transistor  $M_0$  turns off and the four switches  $S_{1-4}$  turn on, making the latch nodes  $X_{1,2}$  and  $O_{1,2}$

charge to  $V_{DD}$ . The decision phase begins at  $t = t_0$  when  $clk$  goes high. Transistor  $M_0$  turns on and biases the input pair transistors  $M_{1,2}$ . Since the input voltage is differential, these devices feed the latch stage with a differential current, which begins discharging nodes  $X_{1,2}$  to zero at different speeds. The latch is then triggered and operates as a strong positive feedback loop to amplify the differential voltage and regenerate outputs to logic levels with an exponential charging speed.

Each decision process is then followed by a reset phase to initialize the outputs to  $V_{DD}$ , making the comparator outputs toggling back and forth between decision and reset values. To retrieve static outputs, the latch comparator is usually connected to a set-reset (SR) latch. Together, these form a comparator chain, as shown in Fig. 2. The corresponding input-output characteristic is then obtained by applying a triangular voltage signal to the positive input  $V_{I1}$  and a constant voltage signal  $V_{CM}$  (common mode voltage) to the negative  $V_{I2}$ . In the general case, the input-output characteristic exhibits a window delimited by two trip points,  $V_{TR+}$  and  $V_{TR-}$ . This window can be very small according to the circuit internal configuration and is called hysteresis. The hystere-



**Fig. 3.** Proposed latch comparator for hysteresis control with an analog adjustment voltage  $V_{Ad}$

sis voltage  $V_{HY}$  is then equal to the difference between trip points  $V_{TR+}$  and  $V_{TR-}$ .

The reset and decision phases, including the regeneration process, were discussed in depth in [6]. Also, a thorough analysis of the circuit operating in both reset and decision phases, led to define hysteresis in terms of internal capacitors and initial voltage levels. For simplicity, in all the following developments, it will be assumed that the sampled input remains constant during the decision process and the circuit is perfectly symmetrical. Also, the total capacitors seen at nodes  $X_{1-2}$  will be assumed equal and denoted by  $C_X$ . Likewise, capacitors seen at nodes  $O_{1-2}$  will be assumed equal and referenced by  $C_O$ . The initial voltages at nodes  $X_{1-2}$  and  $O_{1-2}$  will be denoted by  $V_{0X1,2}$  and  $V_{0O1,2}$ , respectively. The hysteresis voltage  $V_{HY}$  is then a function of the initial voltage differences  $\Delta V_{0X} = V_{0X1} - V_{0X2}$  and  $\Delta V_{0O} = V_{0O1} - V_{0O2}$  and may be written as [6]

$$V_{HY} = f(C_X, \tau) \Delta V_{0X} + g(C_O) \Delta V_{0O}, \quad (1)$$

where  $\tau$  is the time constant of  $X_{1,2}$  discharging, while  $f$  and  $g$  are two positive and nonlinear functions of  $\tau$ ,  $C_X$  and  $C_O$ . The time constant  $\tau$  is a function of the total capacitor  $C_X$  seen at node  $X_{1,2}$ , as well as the gate-drain capacitor  $C_{IX}$  and the on resistance  $r_{o1,2}$  of the input pair transistors. It is defined as

$$\tau = r_{o1,2} (C_{IX} + C_X). \quad (2)$$

To achieve effective hysteresis control, one of the initial voltage differences  $\Delta V_{0X}$  and  $\Delta V_{0O}$  should be kept constant while adjusting the other one. In [17],  $\Delta V_{0X}$  was maintained at near 0 V values while adjusting  $\Delta V_{0O}$ . This required the use of an advanced comparator structure, called the two-stage dual-clock latch comparator, which should be controlled by a specific clock delay circuit, leading to a significant increase in the design complexity. Moreover, the presented technique consisted of

a digital hysteresis adjustment from  $200 \mu\text{V}$  to  $17 \text{ mV}$ , with an average control step greater than  $2 \text{ mV}$ .

Alternatively,  $\Delta V_{0O}$  can be maintained at near 0 V values while adjusting  $\Delta V_{0X}$ , as achieved in [16]. This technique allowed adjustment of hysteresis with good accuracy. However, it was achieved by adjusting device dimensions, and no external control was possible, preventing any accurate compensation of fabrication mismatches.

In general-purpose use, where hysteresis is not of any importance for the application, the reset time is set long enough to charge all the latch nodes  $X_{1,2}$  and  $O_{1,2}$  to  $V_{DD}$ . This makes  $\Delta V_{0X}$  and  $\Delta V_{0O}$  very small, leading to almost cancelling hysteresis. On the other hand, reducing the reset time will not allow controlling hysteresis. Indeed, since  $\Delta V_{0X}$  and  $\Delta V_{0O}$  have opposite signs [6], they may compensate for each other in (1), resulting in an insignificant hysteresis change.

### 3 Proposed latch comparator with accurate hysteresis control

The proposed design of the latch comparator with accurate hysteresis control, is shown in Fig. 3. It includes a hysteresis control circuit consisting of four PMOS transistors  $M_{7-10}$  and one external input, allowing to supply an analog voltage  $V_{Ad}$ . When analyzing this circuit,  $\Delta V_{0O}$  is also maintained constant at near 0 V values, while adjusting  $\Delta V_{0X}$ . There is no specific device sizing except that the channel width of transistors  $S_{1,2}$  should be slightly enlarged with respect to that of transistors  $S_{3,4}$  to make  $\Delta V_{0O}$  reach 0 V before  $\Delta V_{0X}$  during the reset process. In addition, the reset time should be set just long enough to make  $\Delta V_{0O}$  reaching a few tens of millivolts. Thus,  $\Delta V_{0X}$  can be used to adjust  $V_{HY}$  according to (1).

This circuit operates over the two phases, reset and decision, similarly to the basic comparator, except for nodes  $X_{1,2}$ . These nodes are not initialized to  $V_{DD}$  as in basic dynamic comparator. Indeed, at the end of the decision

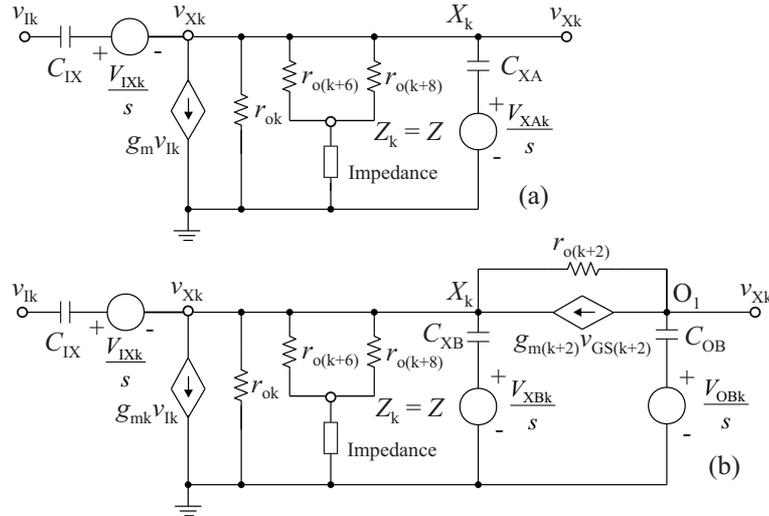


Fig. 4. Small signal equivalent model of the comparator half circuit operating: (a) – in phase A, (b) – in phase B

phase, both  $X_{1,2}$  are at 0 V. With gates tied to the ground, transistors  $M_{9,10}$  are always conducting, making nodes  $Z_{1,2}$  also 0 V. This puts all the source and drain terminals of transistors  $M_{7-10}$  at 0 V, which means that all the drain-source voltages are very small. Thus, at the end of the decision process, the four transistors  $M_{7-10}$  enter triode operation.

When  $clk$  goes low, transistors  $S_{3,4}$  turn on and begin charging nodes  $Z_{1,2}$  to  $V_{DD}$ . Since transistors  $M_{7-10}$  operate in the triode region, nodes  $X_{1,2}$  also charge through transistors  $M_{7-10}$  until nodes  $Z_{1,2}$  reach  $V_{DD} - |V_{THP}|$ . At that point, when the adjustment voltage is set to 0 V, the source-gate voltages of the four PMOS devices  $M_{7-10}$  reach the threshold voltage, making all four transistors enter weak inversion then cutoff. The triode operation followed by the weak inversion and the cutoff of the control devices  $M_{7-10}$  slow down the charging process of nodes  $X_{1,2}$ , with almost no effect on the charging speed of nodes  $O_{1,2}$ .

To analyze the latch comparator, and determine a mathematical expression for its hysteresis, the equivalent small signal models will be used for the two half circuits during decision operation. More specifically, the equivalent circuit of the latch comparator should be drawn twice: before and after transistors  $M_{3,4}$  turn on. This allows considering operations during two consecutive phases, A (before  $M_{3,4}$  turn on) and B (after  $M_{3,4}$  turn on).

When drawing the equivalent circuit using transistors' models, a first simplification may be made by considering nodes  $Z_{1,2}$  as virtually connected to one node  $Z$ . Indeed, the decision phase begins with the four source-drain voltages  $v_{SD7,8} = v_{Z1,2} - v_{X2,1}$  and  $v_{SD9,10} = v_{Z1,2} - v_{X1,2}$  of transistors  $M_{7-10}$  equal to  $|V_{THP}|$ . Thus, as the drain terminals ( $X_{1,2}$ ) discharge to 0 V at different rates ( $v_{X1} \neq v_{X2}$ ), these transistors rapidly enter saturation. As a result, the small difference between  $v_{SD7,8}$

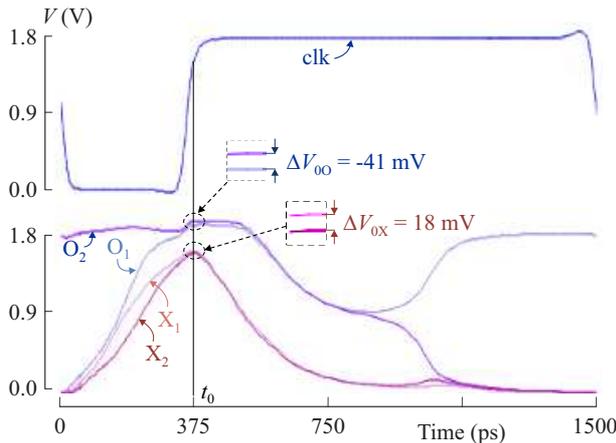
and  $v_{SD9,10}$  due to the fact that  $v_{X1} \neq v_{X2}$ , may occur with almost the same values of  $v_{SG7,8} \approx v_{SG9,10} = v_{Z1,2} - v_{G7-10} = v_{Z1,2}$ . This justifies the assumption that nodes  $Z_{1,2}$  are virtually connected to one single node  $Z$ .

A second simplification may also be made by considering that the saturation operation of the four transistors  $M_{7-10}$  is very brief and that they mainly operate in triode region during the two phases A and B. Indeed, as the current decreases exponentially during any discharging process, transistors  $M_{7-10}$  quickly enter triode operation before transistors  $M_{3,4}$  turn on. Therefore, they are represented only by their respective on-resistances  $r_{o7-10}$ , in both phases A and B when drawing the equivalent model as shown in Fig. 4.

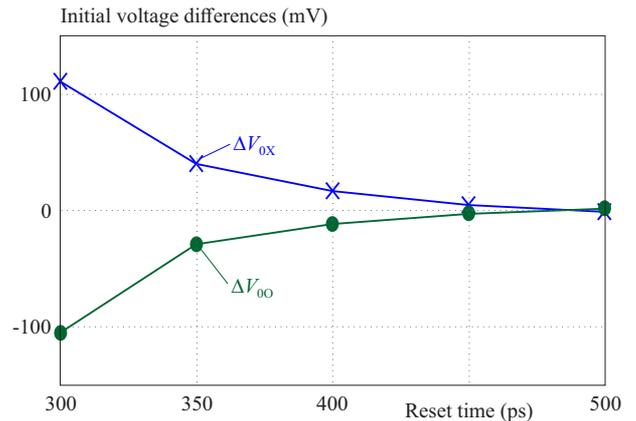
The index  $k$  in Fig. 4 can be replaced by either 1 or 2 to refer to either the left or the right half circuit, respectively. Capacitor  $C_{IX}$  is the gate-drain capacitor of the input transistors.  $V_{IXk}$ ,  $V_{XAk}$ ,  $V_{XBk}$  and  $V_{OBk}$  are the initial charging voltages retrieved from capacitors  $C_{IX}$ ,  $C_X$ , and  $C_O$ , respectively, during phases A and B according to specified indexes. They are represented in Laplace domain with the Laplacian  $s$  as static voltage sources, put in series with the corresponding discharged capacitors.

Analysis of each equivalent circuit leads to determine the output expressions in each phase as well as the differential gain. These results allow extracting the expression of the hysteresis voltage  $V_{HY}$ . It may be easily demonstrated that solving for the outputs in each equivalent model and following the same steps of the analysis methodology given in [6], leads to the following hysteresis expression

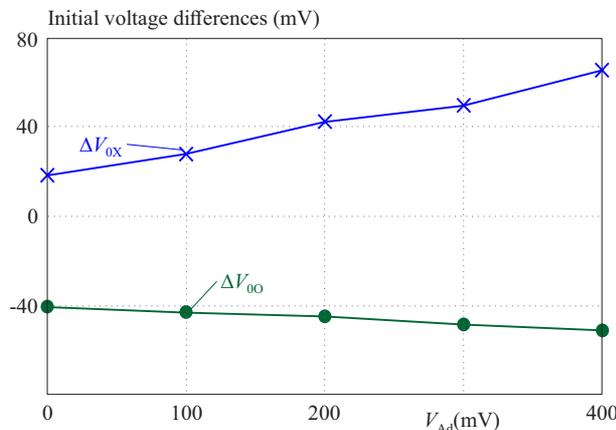
$$V_{HY} = \frac{2}{C_{int}} \left( \frac{C_{IX} + C_{XB}}{C_{int}} \exp \frac{-t_{c1}}{\tau} \Delta V_{0X} + \frac{C_{OB}}{C_{int}} \Delta V_{0OB} \right), \quad (3)$$



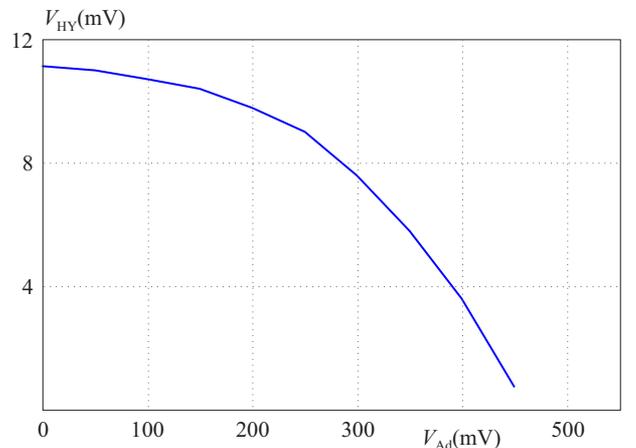
**Fig. 5.** Transient evolution of nodes  $X_1$  and  $O_{1,2}$  in the proposed circuit for  $\Delta V_{IN} = V_{TR-}$ .



**Fig. 6.** Initial voltage differences  $\Delta V_{0X}$  and  $\Delta V_{0O}$  variation in term of the reset time for  $V_{Ad} = 0$



**Fig. 7.** Initial voltages  $\Delta V_{0X}$  and  $\Delta V_{0O}$  variation in term of the adjustment voltage  $V_{Ad}$



**Fig. 8.** Hysteresis voltage  $V_{HY}$  variation in term of the adjustment voltage  $V_{Ad}$

where  $C_{int}$  is defined as

$$C_{int} = C_{IX} \left( \frac{C_{IX} + C_{XB}}{C_{IX} + C_{XA}} \exp \frac{-t_{c1}}{\tau} + 1 \right). \quad (4)$$

$C_{XA}$  and  $C_{XB}$  are the total capacitors seen at nodes  $X_{1,2}$  in phases A and B, respectively,  $C_{OB}$  is the total capacitor seen at node  $O_{1,2}$  in phase B, and  $t_{c1}$  is the time when transistors  $M_{3,4}$  turn on.

Expression (3) may be rewritten in the form of (1) as follows

$$V_{HY} = f(C_{XA}, C_{XB}, \tau_p) \Delta V_{0X} + g(C_{OB}) \Delta V_{0O}, \quad (5)$$

where  $f$  and  $g$  are the same functions as in (1) and  $\tau_p$  is a function of the on resistances  $r_{o1,2}, r_{o7,8}$  and  $r_{o9,10}$  of transistors  $M_{1,2}, M_{7,8}$  and  $M_{9,10}$ , respectively, as

$$\tau_p = (r_{o1,2} || r_{o7,8} || r_{o9,10}) (C_{IX} + C_{XA}). \quad (6)$$

Assuming the triode operation, and having transistors  $M_{7,8}$  controlled by  $V_{Ad}$ , the corresponding on resistances  $r_{o7,8}$  can be written in term of  $V_{Ad}$  as

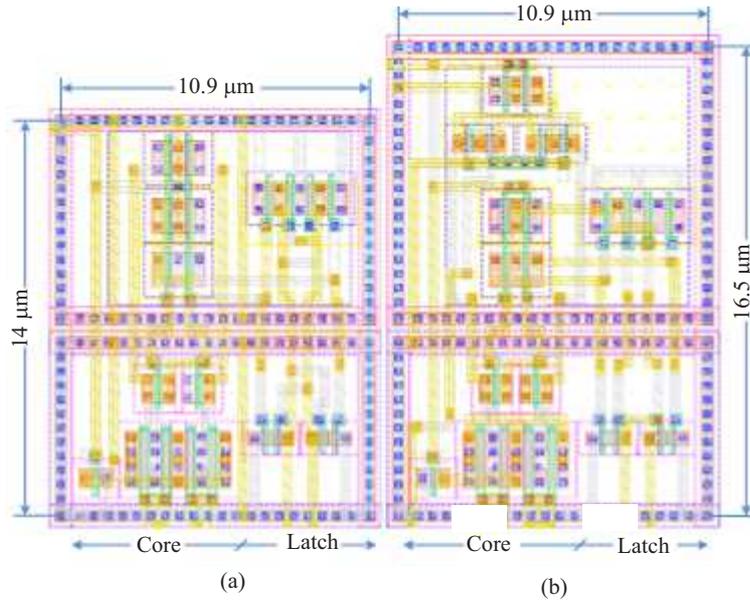
$$r_{o7,8} = \frac{L_{7,8}}{K'_p W_{7,8} (V_Z - V_{Ad} - |V_{THP7,8}|)}. \quad (7)$$

Thus, increasing the adjustment voltage  $V_{Ad}$  increases the on resistances  $r_{o7,8}$ , which increases the total resistance seen at nodes  $X_{1,2}$  and further increases the charging time of nodes  $X_{1,2}$ . In this way,  $\Delta V_{0X}$  can be adjusted using  $V_{Ad}$  only, without affecting  $\Delta V_{0O}$ .

The similarity between the theoretical hysteresis expressions (1) and (3) of the basic and the proposed configurations shows that the proposed configuration allows hysteresis control while preserving the inherent influence of the circuit properties on hysteresis variation.

#### 4 Computer-based analysis of the new latch comparator

The mathematical analysis developed in previous section has required some simplification based on several assumptions. Computer-based analysis including functional simulations of the circuit may be used to assist the theoretical analysis and to confirm the relevance of the assumptions made. Such simulations may also help understanding the circuit operation as stated before. Therefore,



**Fig. 9.** Layout design: (a) – the basic comparator, (b) – the proposed comparator with accurate hysteresis control

**Table 1.** Transistor sizing in the basic and proposed comparators

Parameter	$W$ ( $\mu\text{m}$ )	$L$ ( $\mu\text{m}$ )
$M_0$	0.7	0.18
$M_{1,2}$	4	0.28
$M_{3,4}\&S_{3,4}$	1	0.18
$M_{5,6}\&S_{1,2}$	1.2	0.18
$M_{7-10}$	0.6	0.18

the new latch comparator with accurate hysteresis control proposed in Fig. 3 is simulated using a commercially available 180 nm CMOS process with 1.8 V supply voltage. The clock period is set to 1.5 ns, with an off time (reset time) equal to 350 ps. The input common mode voltage  $V_{CM}$  is set to 1.2 V. Figure 5 shows the resulting transient evolution of nodes  $X_{1,2}$  and  $O_{1,2}$  for an adjustment voltage  $V_{Ad} = 0$  V. The initial voltage differences  $\Delta V_{0X}$  and  $\Delta V_{0O}$  are then equal to 18 mV and  $-41$  mV, respectively.

As stated before, the appropriate reset time corresponds to the value where  $\Delta V_{0O}$  reaches a few tens of millivolts. For a fixed clock period equal to 1.5 ns,  $\Delta V_{0X}$  and  $\Delta V_{0O}$  are determined by simulations while varying the reset time from 300 ps to 500 ps. The obtained results given in Fig. 6, show that the initial voltage difference  $\Delta V_{0X}$  reaches tens of millivolts when the reset time ranges from 350 ps to 400 ps. Therefore, in the remaining simulations the reset time will be set to an average value of 375 ps.

To determine the sensitivity of  $\Delta V_{0X}$  and  $\Delta V_{0O}$  to  $V_{Ad}$  variation, as stated in the interpretation of (5), simulations are performed while varying  $V_{Ad}$  from 0 to 400 mV. The resulting values are reported in Fig. 7 showing a noticeable variation of  $\Delta V_{0X}$  compared to  $\Delta V_{0O}$ ,

which corresponds to the desired operation. This should allow effective control of hysteresis by adjusting  $V_{Ad}$ .

Finally, Fig. 8 shows the hysteresis variation in term of  $V_{Ad}$  for the same simulation configuration. The curve follows a concave down decreasing exponential shape so that a large variation of  $V_{Ad}$  from 0 V to 150 mV, for example, creates a small variation of hysteresis from 11.13 mV to 10.4 mV (range of 0.73 mV), respectively, leading to a very accurate control over hysteresis values that may be linearized to  $4.9 \mu\text{V}/\text{mV}$ . The worst accuracy is obtained with the highest values of  $V_{Ad}$ , where a variation of  $V_{Ad}$  from 400 mV to 450 mV, for example, creates an hysteresis change from 3.6 mV to 0.75 mV (range of 2.85 mV), respectively, which may be linearized to  $57 \mu\text{V}/\text{mV}$  a value that is still highly accurate.

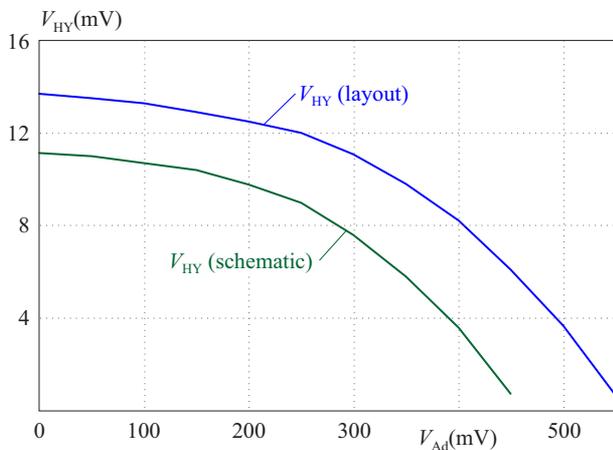
## 5 Implementation and results discussion

Since we are dealing with performances that are tightly dependent of the parasitics, it is appropriate to evaluate the results with post-layout simulations. For that reason, the proposed latch comparator with accurate hysteresis control shown in Fig. 3 is implemented with a commercially available 180 nm CMOS technology using standard-threshold MOS devices. The basic dynamic comparator given in Fig. 1 is also implemented using the same technology and will be used as a comparison basis to evaluate the price to be paid against getting accurate control of the comparator hysteresis instead of settling for the hysteresis which would appear on the circuit. Figure 9 shows the physical implementation of both comparators, while Tab. 1 gives the dimensions of the used devices. In each circuit, the core comparator is followed by an SR latch stage to retrieve static output waveforms, as mentioned previously in Fig. 2.

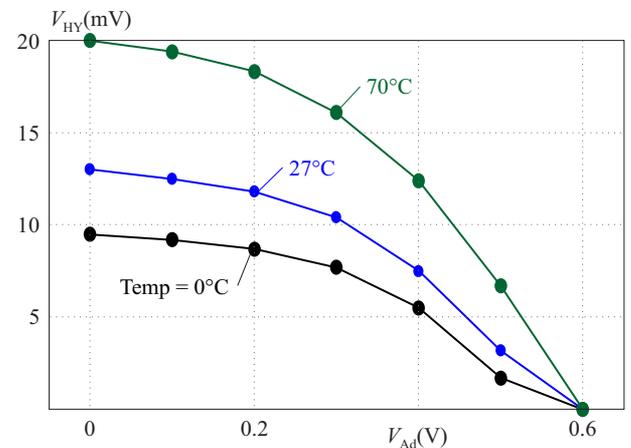
**Table 2.** Characteristics summary and comparison of comparators with adjustable hysteresis

Parameter	2009' [10]	2009' [18]	2016' [19]	2016' [16]	2018' [17]	2020' [20]	This work
Process	CMOS	FGMOS	BiCMOS	CMOS	CMOS	CMOS	CMOS
	0.18 $\mu\text{m}$	0.5 $\mu\text{m}$	9 HP	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$
Technology	Static	Static	Static	Dynamic	Static	Dynamic	Dynamic
Control	Digital	Digital	Digital	W/L <sup>a</sup>	W/L <sup>a</sup>	Digital	Analog
Meas/Sim	Measured	Simulated	Simulated	Simulated	Measured	Simulated	Simulated
Supply (V)	1.8–3.3	3–3.5	1	1.8	$\pm 1.65$	1.8	1.8
$V_{HY}$ range (mV)	51–171 <sup>b</sup>	0–15	0–30	0–18 <sup>b</sup>	$< 800$	0.2–34 <sup>b</sup>	0–39 <sup>b</sup>
Accuracy (mV) <sup>c</sup>	30	–	1.6	$< 0.1$	–	2.2	$< 0.1$
Frequency (Hz)	50	$< 70$	–	800 M	5 M	500 M	650 M
Energy (J/Conv)	204 n	170 n	18.22 p	116 f	562 p	1.15 p	140 f

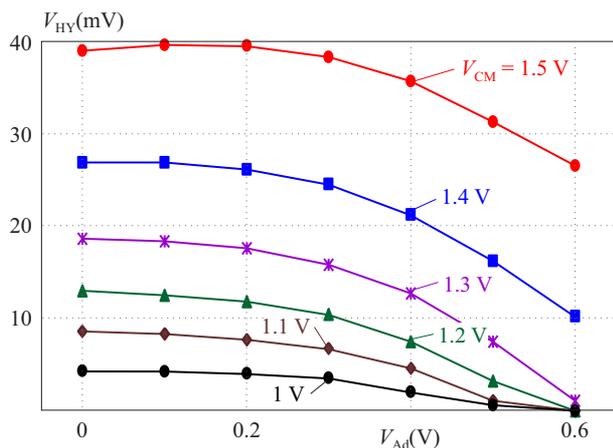
<sup>a</sup> Geometry-based control, <sup>b</sup>  $V_{CM} = 1.5$  V, <sup>c</sup> Average value



**Fig. 10.** Circuit level versus physical level simulation results of the hysteresis variation of the proposed latch comparator



**Fig. 12.** Post-layout simulation of  $V_{HY}$  as a function of  $V_{Ad}$  and temperature



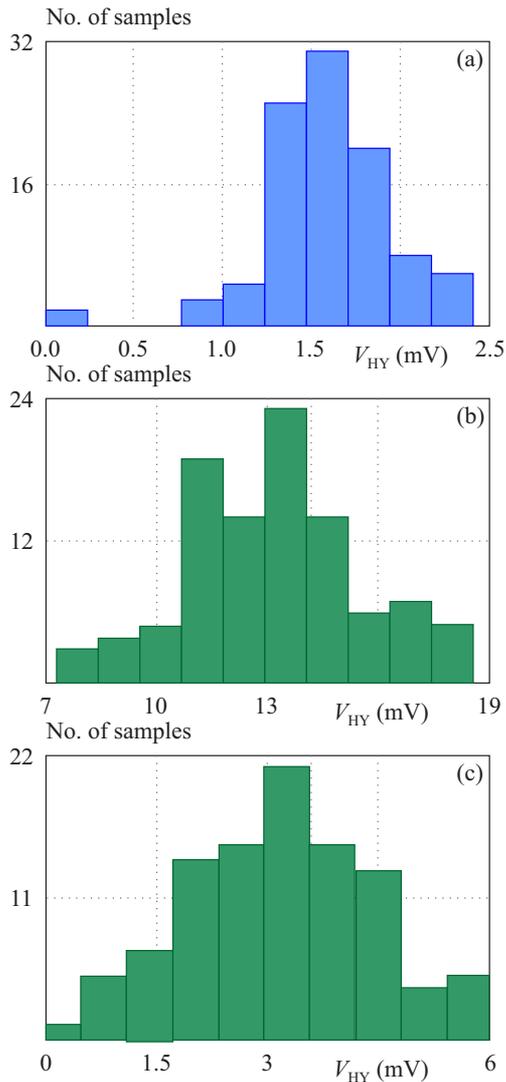
**Fig. 11.** Post-layout simulation of  $V_{HY}$  as a function of  $V_{Ad}$  and  $V_{CM}$

The resulting layout shows that the proposed new design presents an 18% increase in the silicon surface area occupied, going from  $152.6 \mu\text{m}^2$  for the basic comparator to  $180 \mu\text{m}^2$  for the new comparator, which is very reasonable and does not constitute a significant disadvantage.

The physical implementation of the two circuits is then simulated under 1.8 V supply voltage using a 650 MHz clock frequency, for which the reset time was set to 450 ps and 375 ps for the basic and the proposed circuits, respectively. A triangular voltage signal with a small slope and a constant voltage  $V_{CM}$  are applied to the positive and the negative comparator inputs, respectively.

The two comparators are first simulated at room temperature, under nominal conditions and for  $V_{CM} = 1.2$  V. The basic comparator circuit exhibits an hysteresis voltage equal to 1.3 mV, while the proposed latch comparator presents an hysteresis ranging from 14 mV to almost 0 V. Figure 10 shows the schematic and post-layout simulation results of the hysteresis voltage  $V_{HY}$  evolution in term of the adjustment voltage  $V_{Ad}$ . The hysteresis voltage is increased by about 2 mV with respect to schematic simulations for all simulated  $V_{Ad}$  values. This slight increase is mainly caused by the increased capacitor  $C_X$  in (3), which in this case includes all parasitics.

To push further the performance evaluation of the two comparators, the physical implementations are simulated while considering Voltage, Temperature and Process (VTP) variations.



**Fig. 13.** Monte carlo simulation of  $V_{HY}$  (a) – basic comparator (b) – proposed comparator with  $V_{Ad} = 0$  V (c) – proposed comparator with  $V_{Ad} = 500$  mV

The two comparators are first simulated for  $V_{CM}$  ranging from 1 V to 1.5 V, at room temperature and nominal conditions. For the basic comparator, the hysteresis was found equal to 1.2 mV and almost independent of  $V_{CM}$  variation. For the proposed comparator, Fig. 11 shows the hysteresis evolution in term of  $V_{Ad}$ . The proposed design is then sensitive to  $V_{CM}$  variation. This sensitivity may be used to increase the range of hysteresis control.

Second, simulations are performed while varying the temperature from 0 to 70 °C, for fixed  $V_{CM} = 1.2$  V, and at nominal conditions. For the basic comparator, once again, the hysteresis remains almost insensitive to temperature variation. For the proposed one, Fig. 12 depicts the hysteresis evolution. The highest sensitivity is obtained for the highest hysteresis levels when  $V_{Ad}$  is equal to 0 V. This sensitivity decreases with the hysteresis level and is almost null when  $V_{Ad}$  is equal to 600 mV. Since, hysteresis variation remains in the same order of magnitude of the nominal values,  $V_{Ad}$  and  $V_{CM}$  can be used to

compensate for temperature variation and set hysteresis back to any desired nominal value.

Finally, Fig. 13 presents the results of 100 iterations of Monte Carlo post-layout simulation for the two comparator circuits, using  $V_{CM} = 1.2$  V at room temperature. The smallest standard deviation of the hysteresis voltage is obtained for the basic comparator and is equal to 0.4 mV. For the proposed comparator circuit, these runs are performed twice, while setting  $V_{Ad}$  to both extreme values, 0 and 500 mV. The hysteresis standard deviation decreases from 2.5 mV to 1.25 mV when  $V_{Ad}$  increases from 0 to 500 mV. Although the proposed design is sensitive to process variation, the hysteresis extreme variations remain in the same order of magnitude as the nominal values. Therefore,  $V_{Ad}$  and  $V_{CM}$  can also be used to compensate for process variations and set hysteresis back to any desired nominal value.

Table 2 lists the achieved performances, compared to current works. The proposed design achieves almost the highest accuracy and energy efficiency while allowing analog hysteresis adjustment. The achieved switching energy is equal to 140 fJ/Comp, which is almost as low as in [16], while ensuring external hysteresis control from 0 to 40 mV with high accuracy.

## 6 Conclusion

This paper presented a new latch comparator with accurate hysteresis control. The proposed circuit allowed adjusting hysteresis from 0 V to 40 mV, while ensuring an accuracy better than  $5 \mu\text{V}/\text{mV}$ . The proposed low-power latch comparator showed high performances compared to the current state-of-the-art achievements in terms of accuracy, power consumption, and silicon area. Moreover, the accurate external hysteresis adjustment, in conjunction with an adequate setting of the input common mode voltage, may compensate for the sensitivity errors to achieve the desired hysteresis control.

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**Leïla Khanfir** was born in Tunis, Tunisia, in 1986. She received the engineering, the Master and PhD degrees in electrical engineering from the National Engineering School of Tunis, University Tunis El Manar (ENIT-UTM), Tunis, Tunisia, in 2010, 2013 and 2018, respectively. She is currently a lecturer in the Department of Electrical Engineering, ENIT-UTM. Her research interests are related to the analysis and design of advanced comparator structures and the development and design of high speed and high-resolution pipeline ADCs.

**Jaouhar Mouïne** was born in Nabeul, Tunisia, in 1965. He received the engineering degree in electrical engineering from the University of Québec at Trois-Rivières, Trois-Rivières, Canada, in 1986, and the Master and PhD degrees in electrical engineering from the University of Sherbrooke, Sherbrooke, Canada, in 1988 and 1992, respectively. In 1994, he joined the Department of Electrical Engineering, University of Sherbrooke, as an assistant professor, and in 2001 became a full professor. From 2003 to 2015, he has been with the Department of Electrical Engineering, National Engineering School of Tunis, Tunis, Tunisia. Currently, he is a full professor at the Department of Electrical Engineering, College of Engineering, Prince Sattam Bin Abdulaziz University, Al-Kharj, Saudi Arabia. His current research interests are related to advanced microsystems and embedded systems including mixed signal VLSI design.