Journal of Electrical Engineering, Vol. 74, No. 6, 2023, pp. 485-491

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PAPERS

Experimental comparison of operational amplifier and voltage sensor-based zero-crossing detector circuits for power electronic converters

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Zero-crossing detection (ZCD) circuits are widely utilized to synchronize power electronics converters with the grid and measure frequency and phase angle. They are usually designed using an operational amplifier (op-amp) or a voltage sensor accompanied by a processing device. The performance profile of these circuits alters depending on many factors, including the input voltage level. An experimental comparison between the two ZCD circuits across various input voltage levels does not appear to be presented in the literature. This work experimentally compares the performance of an op-amp and an isolated voltage sensor-based ZCD circuits, considering their rise/fall latency and precision in detecting the zero-crossing points (ZCPs). The design process and the experimental results demonstrated that the op-amp-based ZCD circuit is susceptible to false and multiple detections of ZCPs and is best suited for relatively low-voltage applications. On the other hand, the voltage sensor-based ZCD circuit allows signal conditioning and is best suited for relatively high voltage applications.

Keywords: AC-AC conversion, grid synchronization, grid-connected converter, operational amplifier (op-amp), phase detection, voltage sensor, zero-crossing detection (ZCD)

1 Introduction

1.1 Motivation and background

Zero-crossing detection (ZCD) is a widely used hardware solution to achieve synchronization between power electronics converters and the grid [1, 2], and to measure frequency and phase angle [3, 4]. ZCD circuits are designed to detect the precise moment at which the AC signal crosses the zero-voltage threshold, providing a crucial reference point. The input to a ZCD circuit is an AC voltage signal, and the output is a pulse signal that is positive in the positive half cycle of the input signal and zero in the negative half cycle of the same input signal, as shown in Fig. 1. In this way, a pulse signal that indicates the state of the AC input signal is generated. This pulse signal can be used in the modulation process to synchronize the triggering pulses of the power switches with the grid and to measure the frequency and phase angle.

ZCD circuits are utilized in various applications involving AC source/load for synchronization. In [5], a ZCD circuit is utilized to synchronize the voltage source inverter with the grid in a static synchronous compensator system. In [6-11], ZCD circuits are used to control and synchronize various topologies of AC-AC converters. In [12-18], ZCD circuits got involved in various other synchronizing applications. They also got involved in frequency and phase angle measurement applications in [3, 4].

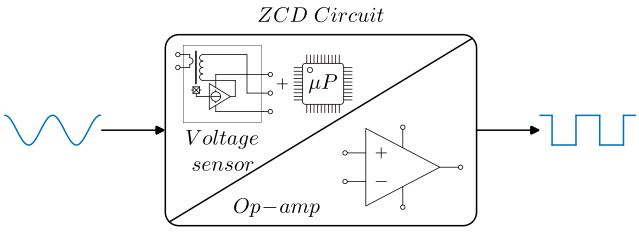

Fig. 1. ZCD circuit working mechanism

1.2 Relevant literature and criticism

ZCD circuits are usually built using optocouplers [5, 11, 19], operational amplifiers (op-amps) [19-23], or voltage sensors [6, 10, 24, 25]. Optocoupler-based ZCD circuits provide the required level of isolation, however, they use diodes that lead to delayed ZCD due to the forward voltage drop. This delay can be compensated with the expense of an additional processing device [19]. Due to these distinct disadvantages, this work does not consider the optocoupler method. Op-amp-based ZCD circuits suffer from false and multiple detections of the zero-crossing points (ZCPs) with distorted input signals. This problem can be solved using different approaches [19]. Nevertheless, these approaches require the use of either additional passive components or a processing device. In [21], an op-amp-based ZCD circuit is proposed that can solve the false and multiple detections of ZCPs, however, it requires the use of additional passive components and a logic integrated circuit. On the other

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https://doi.org/10.2478/jee-2023-0056, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

hand, isolated voltage sensor-based ZCD circuits utilize a relatively low number of passive components while providing the necessary isolation. However, most available rigid sensors are relatively expensive and usually require multiple DC voltage supplies, DC offset, and a processing device to process the sensed input signal. Nevertheless, a processing device comes with the advantage of signal conditioning.

An op-amp-based ZCD circuit that is highly immune from false and multiple detections of ZCPs is proposed in [21]. Nevertheless, the performance of the circuit is not compared with other ZCD methods (e.g., voltage sensor-based), and little attention has been paid to the rise and fall time of the ZCD signal, which is a critical factor, especially in direct AC-AC power conversion applications. The study of [24] analyses the performance of a voltage sensor-based ZCD circuit, however, it fails to perform the analysis at different input voltage levels and to include the op-amp-based ZCD method in the experimental analysis.

1.3 Contributions and organization

In this work, we take a step further to the above literature works by experimentally comparing between op-amp- and isolated voltage sensor-based ZCD circuits. The performances of these circuits are evaluated experimentally at different source voltage levels, considering their rise/fall latency and precision in detecting the ZCPs. To the best of the author's knowledge, this comparison has not been previously reported in the literature. The rest of this paper is organized as follows: in Section 2, the design, along with the strengths and weaknesses points of each ZCD circuit, is discussed. In Section 3, the experimental results are presented and discussed. Finally, in Section 4, the main conclusions of the study are drawn.

2 Circuits design

2.1 Method #1: Op-amp-based ZCD circuit

A general structure of the op-amp-based ZCD circuit is shown in Fig. 2. This circuit is commonly used to trans-fer voltage levels and ensure noise immunity by utilizing fixed hysteresis R_{hs} [19]. The op-amp is used as a comparator, where its positive terminal is connected to the source AC input voltage, and its negative terminal is connected to the ground. The problem with this circuit is that it can detect multiple zero-crossings per fundamental cycle in the case of a distorted input signal. The resistive feedback hysteresis R_{hs} reduces the sensitivity of the op-amp to input noise. However, it results in a phase shift between the AC input signal and the ZCD circuit output signal, faulted frequency and phase angle measurements, and drifting the zero-crossing threshold over the operating temperature range. The hysteresis voltage of the op-amp across its non-inverting terminal is denoted by V_{hs} in Fig. 2.

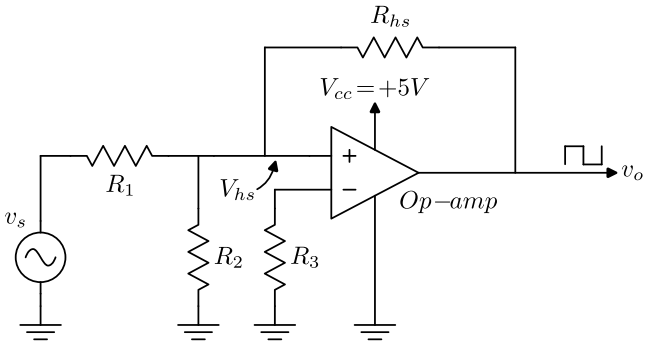

Fig. 2. A general structure of the op-amp-based ZCD circuit with resistive feedback hysteresis

At the ZCPs, the hysteresis voltage can be calculated as per (1).

$$V_{hs} = V_o \frac{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right) + R_{hs}} \tag{1}$$

The circuit output voltage can be represented as in (2).

$$V_o = \begin{cases} 0 & \text{for } V_{hs} < 0 \\ V_{cc} & \text{for } V_{hs} > 0 \end{cases} \tag{2}$$

The voltage lower and higher trip points of the hysteresis can be calculated as per (3) and (4), respectively.

$$V_{LTP} = V_o \frac{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right) + R_{hs}} \tag{3}$$

$$V_{HTP} = V_{cc} \frac{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{\left(\frac{R_1 \times R_2}{R_1 + R_2}\right) + R_{hs}} \tag{4}$$

Therefore, the hysteresis loop width can be calculated as per (5).

$$V_{HLTP} = V_{HTP} - V_{LTP} \tag{5}$$

The higher the noise in the input signal, the higher the hysteresis loop voltage V_{HLTP} should be. Nevertheless, the higher the hysteresis loop voltage V_{HLTP}, the higher the phase difference between the input and output signals and the more faulted measurements.

In this work, the op-amp-based ZCD circuit is constructed without connecting a resistive feedback hysteresis R_{hs} since a passive low pass input filter is used at the input terminals. The circuit is designed using LM358P op-amp. The op-amp V_{cc} is set to +5 V DC.

2.2 Method #2: Voltage sensor with µP-based ZCD circuit

Figure 3 shows a general structure of the voltage sensor with microprocessor (µP)-based ZCD circuit. Voltage sensors require a processing device (e.g., µP) that processes the sensed analog signal to determine the actual values. Sensing the voltage can be performed by stepping down the high voltage to a low level and feeding it to a processing device. However, this initiates safety, isolation, and noise problems. A transformer can be used to provide the required isolation without the need for an external DC power supply, however, it increases the volume of the circuit. Isolated voltage sensors provide a low-voltage analog signal that is isolated from the high-voltage circuit. Nevertheless, most available rigid isolated voltage sensors have the disadvantage of being relatively expensive, and they usually require positive and negative DC voltage supplies. Further, since a digital processing device accompanies the voltage sensor, this increases the cost, complexity, and volume of the ZCD circuit. However, it allows signal conditioning, which is advantageous with distorted inputs [26]. Processing devices usually do not read negative signals. Therefore, a DC offset V_{offset} needs to be added to the sensed signal in order for the processing device to read the positive and negative half cycles of the input AC signal. The processing device can subtract the DC offset V_{offset} or consider it as the zero-crossing line to generate the ZCD signal. Note that most processing devices have voltage limitations (e.g., 3.3 V and 5 V). Consequently, the sensor circuit should be designed keeping these limitations in mind.

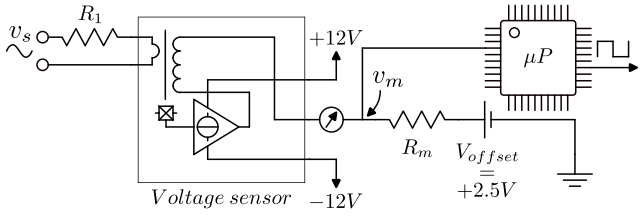

Fig. 3. A general structure of the voltage sensor with µP-based ZCD circuit

In this work, the ZCD circuit of Method #2 is designed using the LEM LV25-P isolated voltage sensor and ATmega328P µP. The voltage sensor produces a current signal that is converter to a voltage by means of R_m. The resistor R_1 controls the input current. The instantaneous voltage that goes to the µP can be represented as in (6).

$$v_m = \frac{v_s}{R_1} k R_m + V_{offset} \quad (6)$$

Here, v_s is the instantaneous source input voltage and k is the current transfer ratio. In this study, +2.5 V DC voltage is connected in series with the output terminals to provide the necessary offset before sending it to the µP, as seen in Fig. 3. The µP processes the analog signal and generates a high (+5 V) pulse if the processed signal amplitude is higher than the DC offset V_{offset} voltage (+2.5 V), and a low (0 V) pulse otherwise. The LV25-P voltage sensor is supplied by ±12 V DC voltages.

3 Experimental comparison

This section presents the experimental comparison results between the two ZCD circuits. The laboratory experimental setup is shown in Fig. 4. The instantaneous source input voltage v_s waveform has a frequency of 50 Hz. The ZCD circuits are tested under 60/120/180/240 V_{rms} source voltages. A variac is used to control the source input voltage level. An input filter of 1.59 kHz cutoff frequency is connected across the variac terminals. Both of the ZCD circuits are supplied from the same filtered source voltage. When harmonics analysis is performed to determine the distortion amount in the filtered source voltage, a total harmonic distortion (THD) of 3.87% is obtained, as shown in Fig. 5. The DC power supply #1 in Fig. 4 is used to supply the op-amp of the ZCD circuit of Method #1, whereas DC power supply #2 is used to supply the voltage sensor of the ZCD circuit of Method #2.

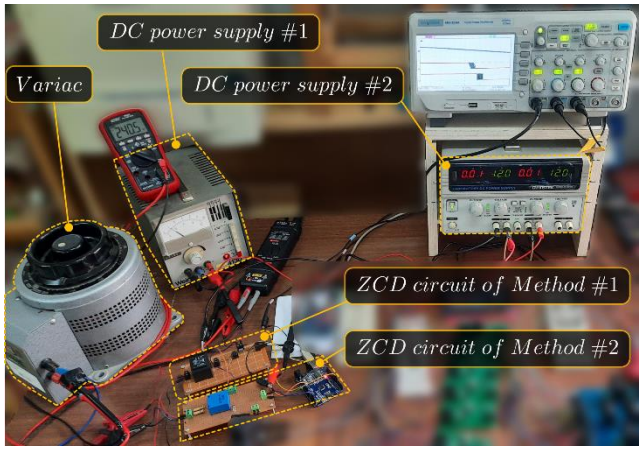

Fig. 4. The experimental setup

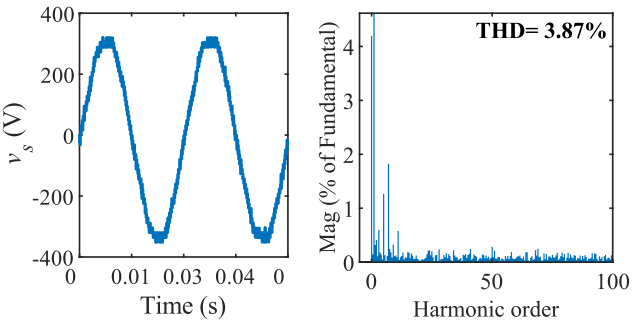

Fig. 5. Source input voltage waveform and its harmonics

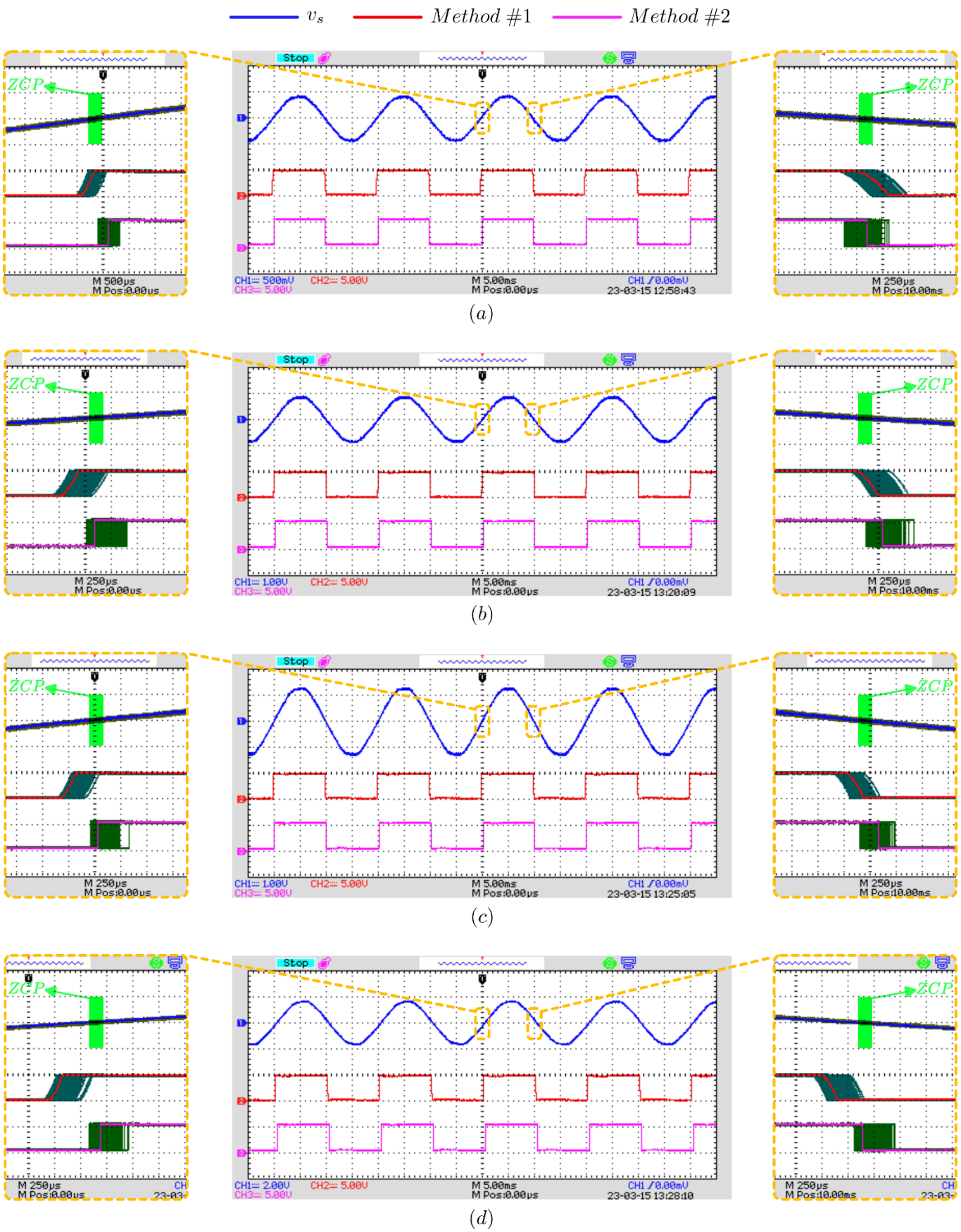

Fig. 6. ZCD signals obtained using Method #1 and Method #2 at source voltages (*a*) 60 V_{rms}, (*b*) 120 V_{rms}, (*c*) 180 V_{rms}, and (*d*) 240 V_{rms}

The input signal is measured using a differential probe, where it is set to X200. A Tech ADS-3204A AA digital storage oscilloscope is used to visualize the source input and the ZCD signals. In order to accurately analyse and judge the performance of each ZCD method, the display intensity in the oscilloscope is set to infinite. Results are captured after one minute. In this way, the performance variation of each ZCD method within one minute is visualized.

3.1 Results and discussion

Figure 6 shows the performance results of the two ZCD circuits at different source voltage RMS values. Note that the values of the blue signal of CH1 (instantaneous source input voltage v_s) are divided by 200 due to the differential probe, as mentioned above. The comparison between the ZCD signals generated by Method #1 and Method #2 reveals notable differences. Specifically, it can be observed that the ZCD signal generated by Method #1 takes approximately 250 µs to gradually rise/fall at the ZCPs. In contrast, the ZCD signal generated by Method #2 exhibits an almost instantaneous rise/fall at the ZCPs. Both methods have shown delayed/hastened ZCD but with different degrees. Looking at the variation of the ZCD signals over one minute from the zoomed-in part of Fig. 6, it is clear that Method #2 has greater precision in rising at the ZCPs than Method #1 for input voltages higher than 120 V_{rms}. Figure 7 compares the latency of the two methods in detecting the ZCPs, where rising is when the input AC signal rises above the zero line to have positive amplitudes and falling is when it falls below the zero line to have negative amplitudes. In Fig. 7, V_s is the RMS value of the source input voltage. It is clear that at rising, Method #2 presents drastically smaller latencies at input voltages higher than and equal to 120 V_{rms}. On the other hand, at falling, Method #2 presents smaller latencies at input voltages higher than and equal to 180 V_{rms} and at 60 V_{rms}. In general, the higher the source input voltage RMS value V_s, the more accurate Method #2 becomes, which is expected due to the limitations of the µP. On the other hand, the higher the source voltage level V_s, the worse the performance of Method #1 becomes. The approximate cost of each ZCD method is given in Tab. 1. The cost of Method #1 is estimated by summing the cost of the op-amp and the other passive components in the circuit. On the other hand, the approximate cost of Method #2 is calculated by summing the voltage sensor, microcontroller, and the other passive components in the circuit. It is clear that the cost of Method #1 is much lower than the cost of Method #2.

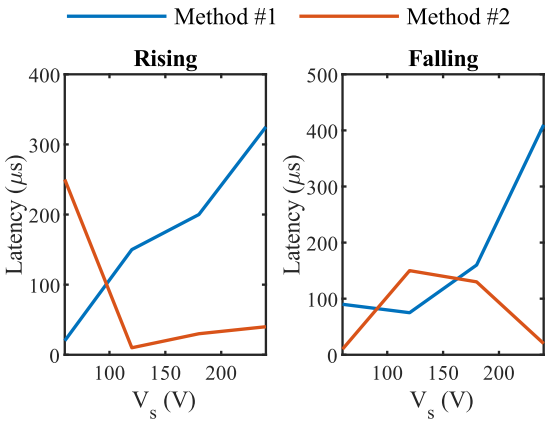

Fig. 7. Latency (delay/haste) in detecting the ZCPs using Method #1 and Method #2

Table 1. Approximate cost of the ZCD circuits

ZCD Method	Cost
Method #1	2 $
Method #2	76 $

4 Conclusion

ZCD circuits play a significant role in synchronizing power electronics converters and measuring frequency and phase angle. These circuits receive an alternating signal and generate a pulse signal that indicates the state of the input signal. The performance characteristics of these circuits may change with the input voltage level. This paper compares the performance of two ZCD circuits that are designed using different methods across various input voltage levels. Method #1 utilizes an op-amp as a comparator, where it compares the alternating input voltage with the ground voltage to generate the ZCD signal. Method #2 utilizes an isolated voltage sensor along with a processing device to generate the ZCD signal. To the best of the author's knowledge, an experimental comparison between the latter two ZCD methods across different input voltage levels is not presented in the literature. In this work, the performance of the ZCD circuits is assessed concerning their latency and precision in detecting the ZCPs. The remarks derived from the design process and experimental results are as follows:

1) Method #1 has a more compact design and requires only one DC power supply. However, it is susceptible to false and multiple detections of the ZCPs with distorted input signals, which results in errored measurements. Addressing this problem requires incorporating passive elements, a processing device, and/or a logic integrated circuit, which increases the circuit volume and makes it vulnerable to environmental variations.
2) Method #2 involves a relatively low number of passive components. However, it requires the use of a process-ing device, two DC power supplies, and a DC offset. Nevertheless, it allows signal conditioning and is less vulnerable to environ-mental variations.
3) At three of the four analysed input voltage levels, Method #2 has demonstrated less latency in detecting the ZCPs at the rising and falling edges of the input AC signal. At input voltages higher than 180 V_{rms}, Method #2 tended to be highly accurate in detecting the ZCPs.

Future work might test the performance of the ZCD methods under more distorted grid voltages.

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Received 2 October 2023