Journal of Electrical Engineering, Vol. 74, No. 6, 2023, pp. 503-512

sciendo

PAPERS

Electrical performance estimation and comparative study of heterojunction strained and conventional gate all around nanosheet field effect transistors

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In this paper, we propose a novel type of Gate All Around Nanosheet Field Effect Transistor (GAA NS FET) that incorporates source heterojunctions and strained channels and substrate. We compare its electrical characteristics with those of the Heterojunction Gate All Around Nanosheet Field Effect Transistor (Heterojunction GAA NS FET) and the Conventional Gate All Around Nanosheet Field Effect Transistor (Conventional GAA NS FET). We investigate the impact of electrostatic control on both DC and analog parameters such as gate capacitance (C_{gg}), transconductance g_m, and cut-off frequency (f_T) for all three device types. In our Proposed GAA NS FET, we employ Germanium for the source and substrate regions, Silicon/Germanium/Silicon (Si/Ge/Si) for the channel, and Silicon for the drain region. The introduction of strain into the nanosheet and the use of a heterojunction structure significantly enhance device performance. Before utilizing a model to analyze a semiconductor device, it is crucial to accurately determine and elaborate on the model parameters. In this case, we solve the Density Gradient (DG) equation self-consistently to obtain the electrostatic potential for a given electron Fermi-level distribution, use the Shockley-Read-Hall (SRH) equation to estimate carrier generation, account for bandgap narrowing in transport behavior, and consider auger recombination. Our general results indicate a notable improvement in drain current, transconductance, and unity-gain frequency by approximately 42%, 53%, and 31%, respectively. This enhancement results in superior RF performance for the Proposed GAA NS FET compared to both the heterojunction GAA NS FET and the conventional GAA NS FET.

Keywords: nanosheet, heterojunction GAA NS FET, conventional GAA NS FET, density gradient, on-state, off-state.

1 Introduction

The scaling down of dimensions and the weakening of electrostatic control in traditional planar bulk devices have led to short channel effects (SCEs) and other undesirable properties in the semiconductor industry. To address these challenges, novel device concepts employing different mechanisms, non-planar structures, or new architectures are required. These new architectures and devices must be developed to overcome adverse effects and enhance channel control [1]. To keep up with Moore's law, various technologies have been proposed to address scaling issues and introduce new layouts. While MOSFET dimensions have continuously shrunk since their inception, this has resulted in an increase in short channel effects (SCEs). However, alterations in fundamental device structures offer potential solutions for achieving high-density chips [2]. Short channel-enabled quantum effects execution a crucial role in determining the transport characteristics of semiconductor systems. As a result, a detailed quantum mechanical treatment of Field-Effect Transistors (FETs) has become increasingly important, especially in the context of scaling theory guiding the roadmap for transistors. Researchers are actively engaged in scaling down FETs, as they believe that reducing the channel length in modified gate devices will lead to improved switching speed and enhanced power-handling capabilities, along with improved linearity [3].

The International Technology Roadmap for Semiconductors (ITRS) emphasizes the need for sophisticated channel engineering methods to scale down Complementary Metal-Oxide-Semiconductor (CMOS) and integrated circuits (ICs) to sub-nanometer sizes. This is because the continuous reduction in device dimensions has led to increased gate leakage current and the emergence of short-channel effects (SCEs) in FETs. Consequently, there has been a growing interest in developing new devices capable of operating at minimal states while keeping SCE levels low in recent years.

In the semiconductor industry, researchers have been exploring new engineering architectures to address the challenges of scaling. These include innovations such as

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https://doi.org/10.2478/jee-2023-0058, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

double gate, gate all around, quadruple gate, dual material double gate, triple material double gate, and nano-sheet FET [4], among others. Simultaneously, efforts have been made to improve electrostatic control and mitigate issues like short-channel effects (SCE), parasitic capacitance, and I_{ON}/I_{OFF} ratio. One limitation encountered with FETs in short-channel designs is the decrease in drive currents due to the reduced effective channel width as devices are downscaled. To overcome these challenges associated with poor electrostatic gate controllability and severe parasitic components, an alternative solution in the form of Gate-All-Around FETs (GAA FETs) has gained prominence in sub-nanometer IC and CMOS technology, potentially replacing Fin FETs [5]. GAA FETs have emerged as promising candidates for transistor scaling after Fin FETs, thanks to their multigate structure, which effectively enhances gate control of the channel, leading to reduced SCE and leakage current. In our study, we integrated 3D stacking technologies with Fin FET and multigate structures, contributing to the ongoing innovations in semiconductor device design.

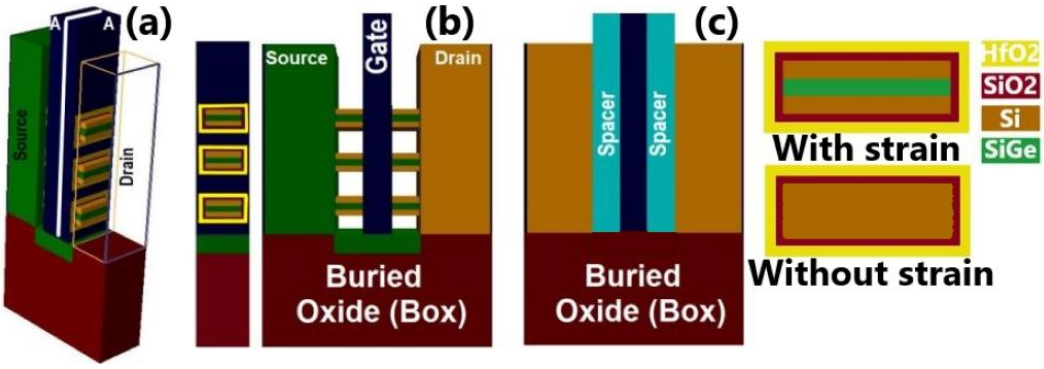

Fig. 1. (a) 3D schematic view of the proposed GAA NS FET, (b) 2D view and cross section of the proposed GAA NS FET, (c) 2D view of Heterojunction GAA NS FET with nitride spacer

Nanosheet FET tech leads the semiconductor industry with a larger channel width and better gate control. It promises to advance logic devices. Semiconductor tech introduces new methods like stack nanosheet, strain engineering, and materials such as high-*k* dielectrics and graphene nanomeshes for improved transistor channels. These innovations are integrated into ICs and CMOS processes, as per the ITRS [6], aiming to enhance both performance and power handling.

One such innovative architecture for the future is the Heterojunction GAA NS FET, which promises high performance technology with improvements in short channel effects (SCE) while maintaining compatibility with existing Fin FET technology and integration. Additionally, further performance gains are anticipated through the manipulation of channel strain [7], as lattice strain presents an effective roadmap for achieving equilibrium in band structures [8, 9]. The dimensions of Nanosheet transistors in nano scale technology nodes are fundamentally similar to those in other nano-scale nodes. Therefore, well calibrated physical models can be effectively applied to device electrical characterization and analog/RF applications in this context [10]. While it is clear that experimental studies of Nanosheet transistors would be more convincing, obtaining nano-scale devices with alternative materials in the substrate for exploring digital/analog RF effects is challenging and limited for comparison purposes. Therefore, we propose exploring various similar structures to provide valuable insights. It has been noted that Heterojunction FETs using Germanium as source and substrate materials have demonstrated enhanced electrical performance [11]. The fabrication process of Gate-All-Around Nanosheet Field-Effect Transistors (GAA NS FETs) has been detailed in previous works [12], involving the epitaxial growth of silicon sheets of varying thicknesses or SiGe in the channels. Experimental verification of the fabrication process and the resulting electrical performance improvements in Gate-All-Around Si Nanosheet Devices have been conducted by researchers such as Zhang et al. [13] and Sun et al. [14]. However, it is worth noting that limited attention has been given to the influence of different materials in the source or drain, oxide thickness, and the impact on digital and analog/RF parameters in NSFETs.

In this study, we conducted simulations on two existing structures and compared them with our proposed structure. One of the effective factors contributing to carrier mobility enhancement was the strain induced by lattice mismatch. To introduce the heterojunction structure and strain engineering into the devices, we employed multilayered Si/Ge/Si materials. The remainder of this paper is structured as follows.

Section 2 provides details on the design, geometry, and simulation methods for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET. Brief discussions regarding potential applications for the proposed device are presented. In Section 3, we delve into the influences of strain engineering and the heterojunction structure on the electrical characteristics of the devices. Section 4 summarizes our key findings.

2 Device structure and simulation method

In Fig. 1, we present schematic views of the three-dimensional (3D) structures of the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET with rectangle cross-section. In the Proposed GAA NS FET, the source region is composed of germanium, while the channels consist of Silicon/Germanium/Silicon (Si/Ge/Si), and the drain region is made of silicon. In contrast, the Conventional GAA NS FET employs silicon for both the source and drain regions, as well as the channels. Additionally, for the Proposed GAA NS FET, a germanium stake substrate has been utilized. Out of various structures considered as candidates to meet these requirements, relaxed silicon (Si) was chosen for the drain regions of both structures, while relaxed germanium (Ge) was selected for the source region of the Heterojunction GAA NS FET. It is worth noting that tensile-strained SiGe plays a crucial role in transforming energy levels within these structures [7]. In our simulations, we utilized a set of parameters for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET, which are summarized in Table 1. Since the channel was of p-type, a metal with a 4.7 eV work function (aluminum) was employed for the gate to generate an internal electric field. This electric field serves to repel electrons from the channel in the OFF state. These parameters include t_{si} (silicon body thickness), W (channel width), and L (channel length). We assumed gate oxide thickness of 0.5 nm for SiO_2 and 1.5 nm for HfO_2. For a comprehensive understanding of the material properties involved, please refer to Table 2. As shown in Fig. 2, the transfer characteristics of the primary structure were compared to those of a reference transfer characteristics curve to calibrate the parameters used in the simulations.

Table 1. Parameters used for devices modeled in this work

Parameter	Proposed GAA NS FET	Heterojunction GAA NS FET	Conventional GAA NS FET
Height of the devices (nm)	60	60	60
Height of the substrate (nm)	30	30	30
Channel material/height (nm)	Strained-Si/2.0 +Relaxed-Ge/1.0 +Strained-Si/2.0	Strained-Si/2.0 +Relaxed-Ge/1.0 +Strained-Si/2.0	Relaxed-Si/5.0
Nanosheet width (nm)	15	15	15
Gate length (nm)	5	5	5
Source/Drain length (nm)	12	12	12
Channel doping (cm^{-3})	p-type 10^{16}	p-type 10^{20}	p-type 10^{20}
Source Drain doping (cm^{-3})	n-type 10^{20}	n-type 10^{20}	n-type 10^{20}
Ge layer of the substrate doping	p-type 10^{16}	-	-
Content of Ge in $Si_{1-x}Ge_x$	x = 0.2	x = 0.2	-
Ge layer L/W/H (nm)	15/15/5	-	-
Spacer dielectric\Underlap (nm)	Nitride\5	Nitride\5	Nitride\5

Table 2. Material properties used in this work (x is the Ge content in the $Si_{1-x}Ge_x$) [7]

Parameter	Equation used
Electron affinity	$X_{Strained-Si} = 4.05 + 0.58x$ $X_{SiGe} = 4.05 - 0.05x$
Band gap energy	$E_{gStrained-Si} = 1.12 - x(0.31 + 0.53x)$ $E_{gSiGe} = 1.12 - 0.42x$
Conduction band offset	$\Delta E_c = 0.63x$
Valance band offset	$\Delta E_V = x(0.74 - 0.53x)$

When dealing with measurements on the scale of nanometers, electron behavior exhibits wave-like characteristics, which are defining features of quantum confinement and tunneling [15]. There are various approaches available for studying quantum transport in such scenarios. One effective approach involves modeling the confinement effects of electrons and holes, which are associated with local potential variations on the scale of electron wave functions (i.e., quantum effects), using a density gradient theory.

It is worth noting that the Density Gradient theory is essentially the same as the Drift-Diffusion (DD) theory, defining a semiconductor as consisting of three components: an electron gas, a hole gas, and a rigid lattice continuum. To improve the accuracy of the Drift-Diffusion equations (DD) when applied to such nano-structures, meticulous quantum corrections are being considered. The Density Gradient (DG) model can be viewed as a direct extension of the Drift-Diffusion (DD) theory, representing a simplified form of quantum corrections. In numerous critical semiconductor devices, quantum physics phenomena, such as electron evanescence, occur within 'quantum wells. These wells are characterized by the imposition of confining potential barriers in one, two, or three dimensions, leading to (quasi) equilibrium conditions [16].

In our simulations, we assumed that the inversion and accumulation layers exhibit behavior similar to an electron gas, undergoing rapid property changes near the interface. To account for quantum confinement effects, we incorporated Density Gradient (DG) quantum corrections for carriers into the simulator. Typically, when solving the density gradient (DG) corrected drift-diffusion (DD) approximation, we employ a modified Gummel approach [17]. This approach entails solving the Poisson equation (1) and the density gradient (DG) equation (2) self-consistently for the electrostatic potential and the quantum-corrected electron density, given a specific electron Fermi-level distribution:

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-) \quad (1)$$

where ψ is the electrostatic potential, ε is the dielectric constant of the material, q is the electronic charge, p is the hole concentration, n is the electron concentration, N_D is the donor concentration and N_A is the acceptor concentration. Equation (2) is the anisotropic density gradient equation, so there are so there are effective mass components in the transport (longitudinal) direction different from those in the confinement (transverse) direction [18].

$$\frac{2b_n^*}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2} + \frac{1}{m_y}\frac{\partial^2 s}{\partial y^2} + \frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right) = \\ = \emptyset_n - \psi\,\frac{k_B T}{q}\ln(S^2) \quad (2)$$

Here $S = \sqrt{n/n_i}$, $b_n^* = \hbar/4qr$, $\emptyset_n$ is the quasi-Fermi level, k_B is the Boltzmann constant, T is lattice temperature and m is the carrier effective mass. The effective quantum-corrected potential is then calculated from equation (3) as follows [18]:

$$\psi_{eff} = \psi + \frac{2b_n^+}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2} + \frac{1}{m_y}\frac{\partial^2 S}{\partial y^2} + \frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right) = \\ = \emptyset_n + \psi + \frac{K_B T}{q}\ln(S^2) \quad (3)$$

which is then used as the driving potential for the current continuity equation:

$$\nabla \cdot J_n = 0 \quad (4)$$

where

$$J_n = -qn\mu_n \nabla \psi_{eff} + qD_n \nabla_n \quad (5)$$

We based our simulations on the effective quantum-corrected potential, which served as the foundation for a Scharfetter-Gummel discretization scheme. We then solved the resulting equations using the 3D ATLAS simulator [19]. To ensure accurate predictions of sub-threshold behavior and Auger recombination, our simulations incorporated the bandgap narrowing model. Additionally, we applied the Shockley-Read-Hall (SRH) model to estimate carrier generation and recombination mechanisms, allowing us to predict doping-induced device properties. Furthermore, Fermi-Dirac (F-D) statistics describing the probability of an electron or hole occupying a certain energy level under equilibrium states was considered [20]. The system of Eqns. (1, 2,

and 4) was solved self-consistently until convergence, with Dirichlet boundary conditions applied at the interface between the source, channel, and drain contacts.

3 Results and discussions

In Fig. 2, we illustrate the drain currents of the Proposed GAA NS FET, Heterojunction GAA NS FET, and the Conventional GAA NS FET as functions of various V_{GS} and $V_{\mathrm{DS}} = 0.6$ V. The graph highlights the ability to control drain current by adjusting the gate voltage, enabling precise regulation and modulation of the transistor's output. It's important to note that the shift in threshold voltage and the variation in drive current, both influenced by applied voltage, have a significant impact on the performance of these structures. The threshold voltage was extracted under a current of 1 μA at various V_{GS} and $V_{DS} = 0.6$ V.

The threshold voltage of a semiconductor device is a crucial parameter that significantly influences its performance. Changes in device structures, such as those involving strain engineering and heterojunction configurations, can lead to variations in the threshold voltage. In the case of the Proposed GAA NS FET, the threshold voltage is notably lower when compared to the Heterojunction GAA NS FET and the Conventional GAA NS FET. The discrepancy in threshold voltage between the Proposed GAA NS FET and the other structures is approximately 12%. This reduction in threshold voltage can be attributed to the decrease in the electric field, which confines fewer carriers closer to the surface. This, in turn, enhances carrier mobility and ultimately results in a lower threshold voltage.

The threshold voltage values for the Proposed structured, Heterojunction GAA NS FET, and Conventional GAA NS FET are tabulated in Tab. 3. In a Field Effect Transistor (FET), the drain current is significantly influenced by the energy bands present in the semiconductor materials that constitute the device. The magnitude of the current flowing through the transistor is intricately tied to the inherent characteristics of the device, including the configuration of energy bands in both active and inactive states. These energy bands play a critical role in determining the accessibility of energy states for charge carriers.

The distinctive graph representing the Proposed structured variant demonstrates a peak in current intensity. This observation becomes particularly pronounced when examining the characteristics that highlight significantly higher drain current levels for the Proposed structured design. The increase in drain current is a result of several factors, including enhanced carrier mobility, increased drive currents, and improved electrostatic performance conductivity. Overall, the Proposed structured design exhibits superior drain current characteristics, featuring higher levels of drain current due to its high carrier mobility, enhanced drive currents, and superior electrostatic performance conductivity when compared to the Heterojunction GAA NS FET and Conventional GAA NS FET.

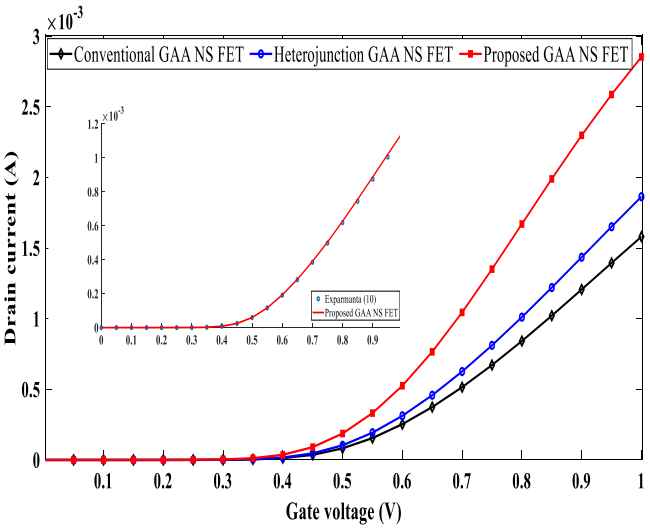

Fig. 2. Drain current of the for Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{\mathrm{DS}} = 0.6$ V

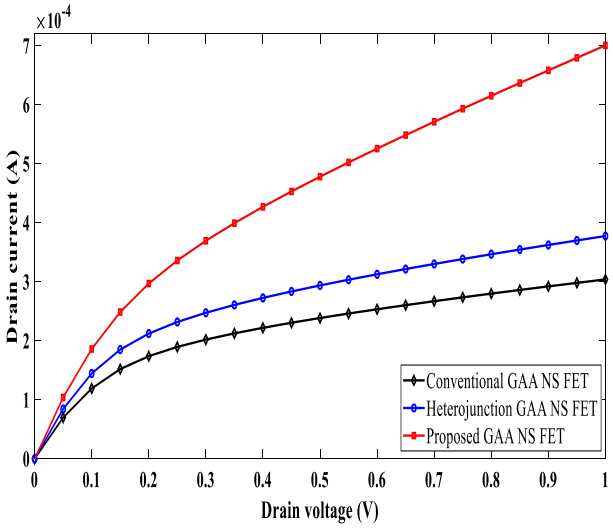

Fig. 3. Variation of drain current for Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{\mathrm{DS}} = 0.6$ V

Table 3. Electrical characteristics of Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET

Parameter	Conventional GAA NS FET	Heterojunction GAA NS FET	Proposed GAA NS FET
V_{th} (V)	0.298	0.281	0.251
I_{ON} (A)	5.06×10^{-4}	5.50×10^{-4}	7.71×10^{-4}
I_{OFF} (A)	2.0×10^{-9}	2.8×10^{-9}	2.8×10^{-9}

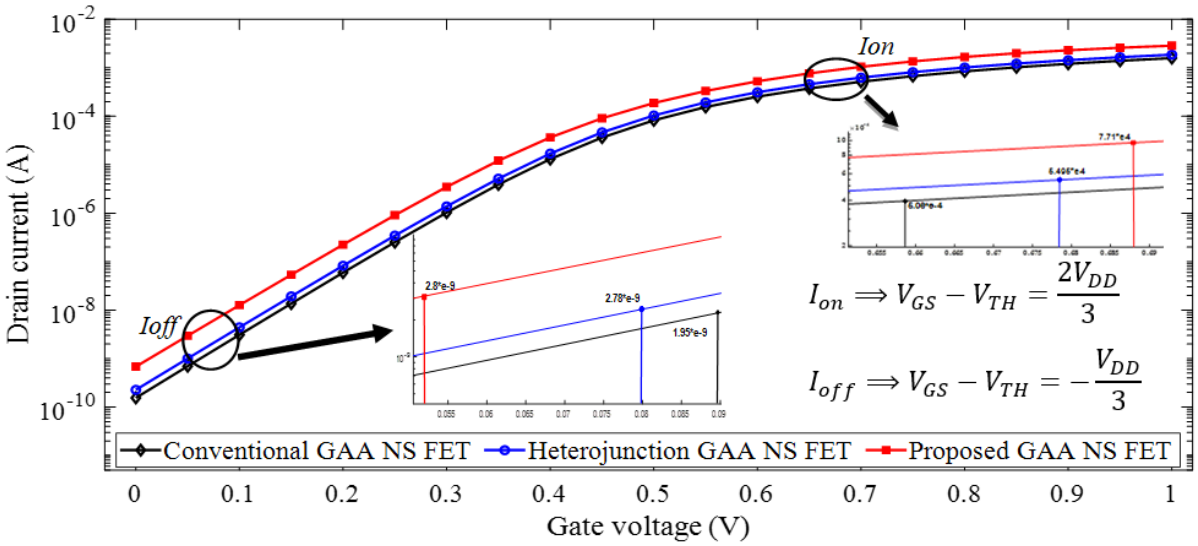

Fig. 4. Drain current of the Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET FET under various V_{GS} and $V_{\mathrm{DS}} = 0.6$ V in logarithmic scale

In Fig. 3, we present the variations in drain current for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET as functions of drain voltage at under various V_{GS}. When drain voltage is applied, charge carriers move through the channel region of the transistor. The flow of these carriers is directly influenced by the electric field within the channel, which, in turn, is determined by the drain voltage. As the V_{DS} increases, more charge carriers attempt to traverse the narrow channel. However, beyond a certain threshold, the drain current saturates, even if the drain voltage continues to rise. This saturation phenomenon can be attributed to strain engineering and the heterojunction structure, both of which enhance carrier transport efficiency by facilitating the movement of more carriers toward the drain side. The curve clearly illustrates that the drain current is more pronounced for the Proposed structured GAA NS FET when compared to its Heterojunction GAA NS FET and Conventional GAA NS FET counterparts.

Table 3 provides the threshold voltage values, determined from the I-V characteristics of the mentioned devices. We define the threshold voltage as the gate voltage at which the drain current reaches 0.1 μA (when various $V_{\mathrm{GS}} = 0$ to 1.0 V and $V_{\mathrm{DS}} = 0.6$ V). Notably, the Proposed structured GAA NS FET exhibits a lower threshold voltage in contrast to both the Heterojunction GAA NS FET and the Conventional GAA NS FET. Additionally, in Tab. 3 one can observe the ON and OFF state currents for all three structures. It becomes evident that the Proposed GAA NS FET offers a higher ON current and a reduced OFF current. Both the ON and OFF state currents for these structures are visualized in Fig. 4. The $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is a crucial criterion for integrated circuits (ICs) and CMOS technology, especially in low-power applications where high-speed operation is a priority [21]. The Proposed GAA NS FET device provides more space at the source-channel for carriers to drift when the transistor is in the ON state. Due to enhanced carrier velocity in the source and the effective channel width, results in a larger on current. Moreover, the conduction band offset energy leads to electrons gaining more kinetic energy, contributing to the higher I_{ON} values. Consequently, the Proposed GAA NS FET exhibits favorable switching characteristics, boasting a significantly higher I_{ON} ratio (approximately 52% and 40.3%) when compared to the Conventional GAA NS FET and Heterojunction GAA NS FET, respecttively.

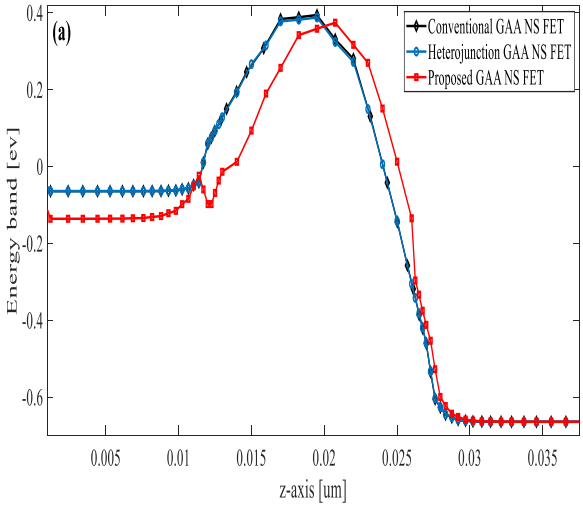

Fig. 5(a). Band diagram in the horizontal direction in the S/D edge region for Proposed GAA NS FET Hetero-junction GAA NS FET and Conventional GAA NS FET in off-state under $V_{GS} = 0$ V and $V_{DS} = 0.6$ V

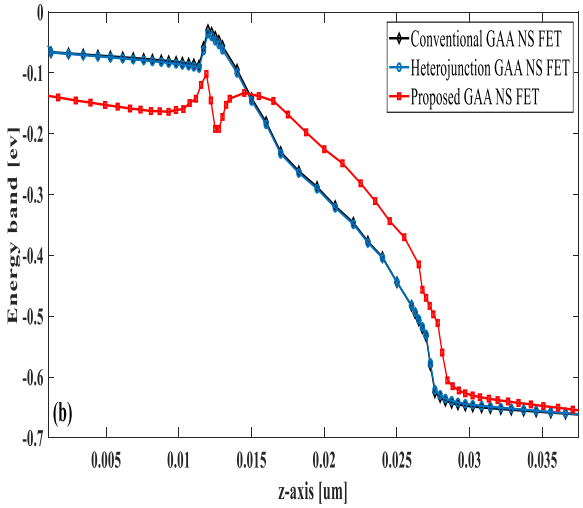

Fig. 5(b). Band diagram in the horizontal direction in the S/D edge region for Proposed GAA NS FET Hetero-junction GAA NS FET and Conventional GAA NS FET in on-state under various V_{GS} and $V_{DS} = 0.6$ V

In the off-state mode, I_{OFF} remains independent of the gate voltage but increases with rising drain voltage, as depicted in Fig. 4 showing a comparative analysis of energy band diagrams in the S/D edge region for the Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET in off-state is shown in Fig. 5(a). In the OFF state, there are insufficient carriers in the source region for injection into the channel for all structures. To achieve high off-state performance, it is crucial to deplete the channel to attain a suitably low off-state current. Applying a positive voltage to the structure generates an electric field that influences the energy bands. This electric field increases the number of carriers transferred to the gate electrode, accumulating them in the layer beneath the gate. As the gate voltage increases, the energy band of the channel undergoes variations, particularly in the flat band region. The presence of electrons in the conduction band directly impacts the electron density, signifying a larger pool of available electrons for conduction.

In the ON-state current, electron velocity and the peak electron velocity near the source region provide increased acceleration to electrons in the channel, contributing to enhanced carrier accumulation and velocity near the gate region, as illustrated in Fig. 5(b). As the gate voltage gradually increases, the presence of the heterojunction structure near the gate becomes more apparent, resulting in pronounced band bending and a stronger electron velocity. Electron carriers can achieve higher drift velocities, enabling them to overcome the barrier width, resulting in a steep increase in the drain current. Fig. 5(b) illustrates this phenomenon. In this context, it is evident that the Proposed GAA NS FET device outperforms both the Hetero-junction GAA NS FET and the Conventional GAA NS FET devices. This superiority can be attributed to the presence of the heterojunction and strained germanium in the substrate region, which significantly enhances carrier transport within the channel of the Proposed GAA NS FET when compared to the Heterojunction GAA NS FET and Conventional GAA NS FET.

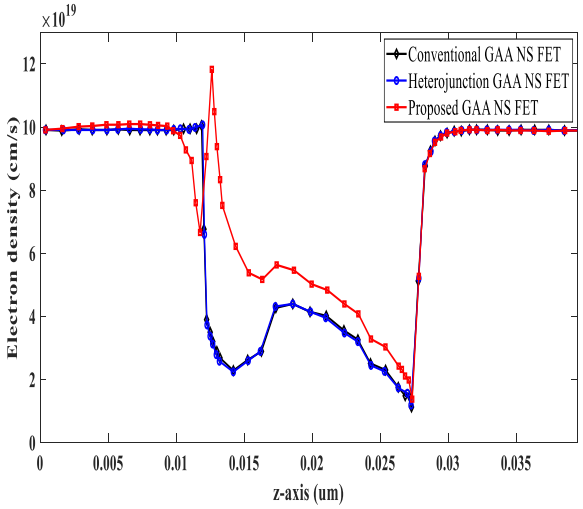

Fig. 6. Electron densities varying with same gate to source voltage for Proposed GAA NS FET, Hetero-junction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{DS} = 0.6$ V

In Fig. 6, we observe the variations in electron densi-ties at various V_{GS} and V_{DS}=0.6 V for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conven-tional GAA NS FET. The graph illustrates dis-tinct stages of electron density in these devices. Notably, in the case of the Conventional GAA NS FET and Heterojunction GAA NS FET, as depicted in Fig. 6, the electron density remains notably lower, indicating an insufficient number of carriers available in the channel

region. The electron density within a material plays a crucial role in determining the abundance of available charge carriers. When an electric field is applied, these charge carriers, typically electrons, respond by acquiring an electric velocity. The magnitude of this drift velocity, and consequently the electron velocity, is influenced by various factors, including carrier mobility, electron density, material properties, temperature, etc. Figure 6 demonstrates that the electron density begins to increase around the gates, leading to the formation of the channel. It is evident that, owing to strain engineering and the unique proposed structure, the control of carrier flow in the Proposed GAA NS FET is superior to that in the other structures.

The electron velocity can be determined using the formula $I = qnvA$, where A represents the cross-sectional area, q denotes the carrier charge, n signifies the electron density (as shown in Fig. 7), and v represents the velocity of electrons. Figure 7 illustrates that the electron velocity within the channel region of the Proposed GAA NS FET is notably higher when compared to both the Heterojunction GAA NS FET and the Conventional GAA NS FET. In the Proposed GAA NS FET, electrons are injected into the channel with a high velocity, thanks to the shift of the conduction band at the source-relaxed SiGe/channel-strained Si hetero-interface. Owing to the influence of strain engineering and the presence of the heterojunction structure, the Proposed GAA NS FET exhibits significant enhancements in electron velocity compared to the Heterojunction GAA NS FET and the Conventional GAA NS FET.

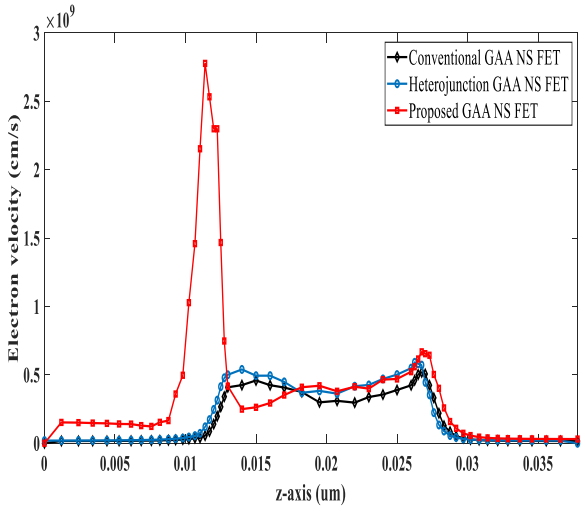

Fig. 7. Electron velocity in the horizontal direction in the S/D edge region for both Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{DS} = 0.6$ V

Following an examination of the electrical characteristics of the devices, the other crucial parameters pertain to analog/RF circuits. When designing analog circuits, key parameters include transconductance g_m, gate capacitance C_{GG} and cutoff frequency F_T.

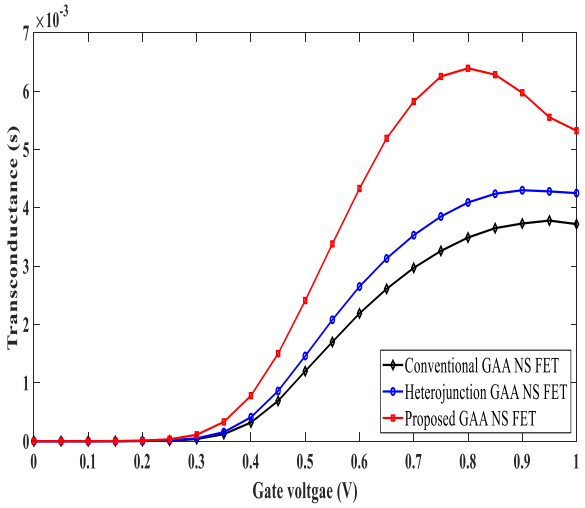

Fig. 8. Transconductance (g_m) characteristics of the Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{DS} = 0.6$ V

Transconductance g_m is a crucial factor for increasing circuit speed and is calculated as $g_m = \partial I_{DS}/\partial V_{GS}$. In Fig. 8, we can observe the transconductance g_m characteristics of the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET at various V_{GS} and $V_{DS} = 0.6$ V at the source-relaxed SiGe/channel-strained Si hetero-interface. A higher g_m in the device indicates better transport efficiency within the channel, a higher voltage gain for analog applications, and faster device performance. As depicted in Fig. 8, the transconductance of the Proposed GAA NS FET surpasses that of both the Heterojunction GAA NS FET and the Conventional GAA NS FET. Gate capacitance C_{GG} directly influences the gate voltage's ability to control charge carrier density in the channel. Variations in drain current induce a displacement of charge carriers within the channel, affecting current flow and resulting in changes in transconductance. This improvement in the transconductance of the Proposed GAA NS FET can be attributed to enhanced electron velocity, leading to increased carrier mobility and reduced channel resistance.

In Fig. 9, we observe the variation in total gate capacitance with respect to gate voltage V_G. The performance of these devices is significantly influenced by the total gate capacitance, which can be enhanced by reducing the C_{GG} value. In heterojunction-strained structures, the gate capacitance can be influenced by two factors: a decrease in the barrier between the source and channel and the accumulation of charges near the hetero-interface.

Among the three structures, capacitance increases as V_{GS} leads to increased propagation delay and reduced circuit performance, resulting in lower switching speeds. However, a source heterojunction strained channel exhibits higher capacitance due to the increased parasitic capacitance area. Notably, the gate capacitance value for the Proposed GAA NS FET is consistently higher than that of both the Heterojunction GAA NS FET and the Conventional GAA NS FET.

The cut-off frequency F_T of the device is influenced by both transconductance g_m and total gate capacitance C_{GG}. In Fig. 10, one can observe the cut-off frequency characteristics of the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET.

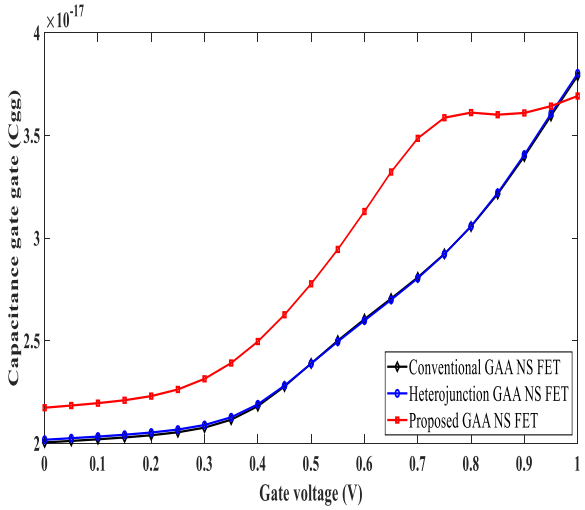

Fig. 9. The total gate capacitance with ac frequency 1 MHz under various V_{GS} and $V_{DS} = 0.6$ V

The cut-off frequency is calculated using the formula $F_T = (g_m/2\pi C_{GG})$. Furthermore, as the drain voltage increases, the device can achieve higher mobility, resulting in an increase in transconductance. It is well-documented that higher transconductance leads to higher cutoff frequencies. The results clearly demonstrate that the Proposed GAA NS FET exhibits a higher cutoff frequency compared to both the Heterojunction GAA NS FET and the Conventional GAA NS FET. This superior performance can be attributed to better gate control and increased transconductance. Optimizing these factors is crucial for enhancing high-frequency device performance, particularly in high-speed applications. The cutoff frequencies for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET are summarized in Fig. 10 when V_{GS} =0.8 V and V_{DS} =0.6 V.

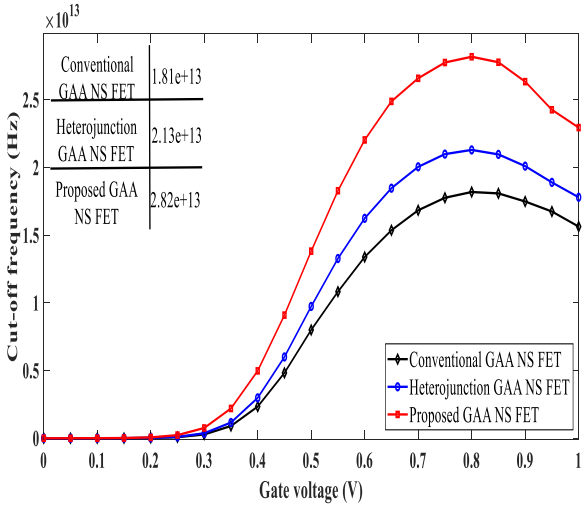

Fig. 10. Cut-off frequency characteristics of the Proposed GAA NS FET, Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{GS} and $V_{DS} = 0.6$ V

4 Conclusion

We conducted a comprehensive analysis of different device performance parameters for the Proposed GAA NS FET, Heterojunction GAA NS FET, and Conventional GAA NS FET devices. By varying the geometrical structure of the nanosheet in the 3D vertically stacked GAA NS FET, we explored the detailed DC/AC performance. The results revealed an increase in parameters as the nanosheet structure was varied. Notably, within the framework of the density gradient model, the Proposed GAA NS FET structure achieved a high on-state current (I_{ON}), surpassing the performance of other structures. Despite its large capacitance, the Proposed GAA NS FET demonstrated a higher cut-off frequency (F_T) compared to both the Heterojunction GAA NS FET and the Conventional GAA NS FET. In summary, our analysis yielded improved characteristics in the Proposed GAA NS FET compared to the other structures. Consequently, the Proposed GAA NS FET holds promise as a high-speed device for down scale applications

References

[1] M. Han, Ch. Chang, H. Chen, Y. Cheng, and Y. Wu, "Device and Circuit Performance Estimation of Junctionless Bulk FinFETs," *IEEE Transaction on Electron Devices*, vol. 60, no. 6, pp.1807-1813, 2013.
doi: 10.1109/TED.2013.2256137

[2] A. S. Rawat, and S. K. Gupta, "Potential modeling and performance analysis of junction-less quadruple gate MOSFETs for analog and RF applications," *Microelectronics Journal*, vol.66, pp.89-10, 2017. doi:10.1016/j.mejo.2017.06.004

[3] S. Milshtein and C. Liessner, "High speed switch using pairs of pHEMTs with shifted gates," *Microelectronics Journal*, vol. 36, pp. 316–318, 2005. doi:10.1016/j.mejo.2005.02.052.

[4] A. Veloso, G. Eneman, A. Keersgieter, D. Jang, H. Mertens, P. Matagne, E. Dentoni, J. Ryckaert, and N. Horiguchi, "Nanosheet FETs and their Potential for Enabling Continued Moore's Law Scaling,"*2021 Electron Devices Technology and Manufacturing Conference (EDTM),* 2021. doi: 10.1109/EDTM50988.2021.9420942.

[5] E. Mohapatra, T. P. Dash, J. Jena, S. Das, and C. K. Maiti. "Strain induced Variability Study in Gate All Around Vertically Stacked Horizontal Nanosheet Transistors,". *Physica Scripta*, vol.95, no. 6, pp. 065808, 2020. doi: 10.1088/1402-4896/ab89f5

[6] H. Park, W. Choi, M. Pourghaderi, J. Kim, U. Kwon, and D. Kim "NEGF simulations of stacked silicon nanosheet FETs for performance optimization," *2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD),* 2019. doi: 10.1109/SISPAD.2019.8870365

[7] S.-T. Chang, "Nanoscale Strained Si/SiGe Heterojunction Trigate Field Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 44, no. 7A, pp. 5304-5308, 2005. doi: 10.1143/JJAP.44.5304

[8] S. Reboh, R. Coquand, N. Loubet, N. Bernier, E. Augendre, R. Chao, J. Li, J. Zhang, R. Muthinti, V. Boureau, T. Yamashita, and O. Faynot, "Imaging, Modeling and Engineering of Strain in Gate All Around Nanosheet Transistors," *2019 IEEE Inter-national Electron Devices Meeting (IEDM)*, 2019. doi:10.1109/IEDM19573.2019.8993524

[9] K. H. Hong, J. Kim, S. H. Lee, and J. K. Shin, "Strain-Driven Electronic Band Structure Modulation of Si Nanowires," *Nano Letters*, vol. 8, no. 5, pp. 1335-1340, 2008. doi:10.1021/nl0734140

[10] N. A. Kumari, and P. Prithvi, "Performance Evaluation of GAA Nanosheet with Varied Geometrical and Process Parameters," *Silicon*, vol. 14, pp. 9821-9831, 2022. doi:10.1007/s12633-022-01695-7

[11] C. Usha, and P. Vimala, "Analytical Drain Current Modeling and Simulation of Triple Material Gate All Around Heterojunction TFETs Considering Depletion Regions," *Semiconductors*, vol. 54, no. 12, pp. 1634-1640, 2020. doi: 10.1134/S1063782620120398

[12] S. Mukesh, and J. Zhang, "A Review of the Gate All Around Nanosheet FET Process Opportunities," *Electronics*, vol. 11, no. 21, pp. 3589 (1-11), 2022. doi: 10.3390/electronics11213589

[13] Q. Zhang and et al., "Optimization of Structure and Electrical Characteristics for Four-Layer Vertically-Stacked Horizontal Gate All Around Si Nanosheets Devices," *Nanomaterials,* vol. 11, no. 6, pp. 664, 2021. doi:10.3390/nano11030646

[14] Y. Sun, X. Li, Z. Liu, Y. Liu, X. Li, and Y. Shi, "Vertically stacked nanosheets tree-type reconfigurable transistor with improved ON-current," I*EEE Transactions on Electron Devices*, vol. 69, no. 1, pp. 370-374, 2022. doi: 10.1109/TED.2021.3126266

[15] O. Talati, and R. Hosseini, "Device and circuit performance simulation of a new nano scale side contacted field effect diode structure," *Journal of Optoelectronical Nanostructures*, vol. 4, no. 3, pp. 17-32, 2019. doi: 20.1001.1.24237361.2019.4.3.2.4

[16] M. Ancona, "Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices," *Journal of Computational Electronics,* vol. 10, no. 1, pp. 65-97, 2011. doi: 10.1007/s10825-011-0356-9

[17] P. Andrei, "Calibration of the Density-Gradient model by using the multidimensional effective-mass Schrödinger equation," *Journal of Computational Electronics,* vol. 5, pp. 315-318, 2006. doi: 10.1007/s10825-006-0013-x

[18] A. Wettstein, Schenk, and W. Fichtner, "Quantum Device Simulation with the Density Gradient Model on Unstructured Grids," *IEEE Transaction on Electron Devices*, vol. 48, pp. 279-283, 2001. doi: 10.1109/16.902727

[19] Atlas User Manual, Device Simulation Software; 2011

[20] A. Richter, S. Glunz, F. Werner, J. Schmidt, and A. Cuevas, "Improved quantitative description of Auger Recombination in crystalline silicon," *Physical Review B*, vol. 86, no. 16, p. 165202, 2012. doi: 10.1103/PhysRevB.86.165202

[21] M. Bavir, A. Abbasi, and A. Orouji, "Dual P^+-Wire Double-Gate Junctionless MOSFET with 10-nm regime for Low Power Applications," *Journal of Electronic Materials*, vol.51, pp. 2083-2094, 2022. doi: 10.1007/s11664-022-09462-5

Received 2 October 2023